



RS740M-M v : B

SCHEMATICS TABLE:

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REVISION HISTORY:

Rev	Date	Notes
A	07-09-2007	INITIAL RELEASE
B		1>Follow Richtek's suggestion: change R137 390 OHM and R136 to 180 OHM 2>Connect VID5 for PWM K8_M2 mode. 3>Add EC41 in BOM and reserve BC48 for 5VSB noise issue 4>Change U10 from 1117 to RT9173 for 1.2VSB 1.2V level. 5>Change ER66 to 210 OHM for VDIMM default value 1.85V 6>Change ER59 to 1.91K for VCC_SB 1.2V level. 7>Add C89 0.1UF in BOM for SB_PWRGD signal abnormity waveform issue 8>Deleted R130 in BOM for VID1 pull up dummy 9>Deleted R72,R73,R74,R75 in BOM to follow new demo board. 10>Deleted BC45,R210,SC67,MC49,BC46,MC43,SC53 for cost and follow new demo board 11>Change C105,C106 from 56PF to 47PF for RTC issue 12>Add SC72 10UF for SATA signal fail issue 13>Connect VBAT_IO with VBAT net. 14>Change SIO JP2 to pull up to enable adjust VDIMM function 15>Change G_LED2 pull up to VCC 16>Change VCC3 to LAN2.5V for SU1 and SU2 17>Add C1,C2 in BOM for Gigabit Lan. 18>Reserve WT_BEEP function 19>Change RJ14 install Pin1->2 to match SB straps 20>Deleted R214,R216,R217 in BOM 21>Change L4,L5,L6 from FB 30 OHM to inductor 68uH to follow demo board 22>Change R195 to 20M 0402 23>ADD RJ18 for TMDS_HPD choice 24>ADD C350,SC73,SC74 for LVTM Power
1.0		1>Modify VGA circuit 2>Modify SB700 VDD Core power circuit for ver:A12

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

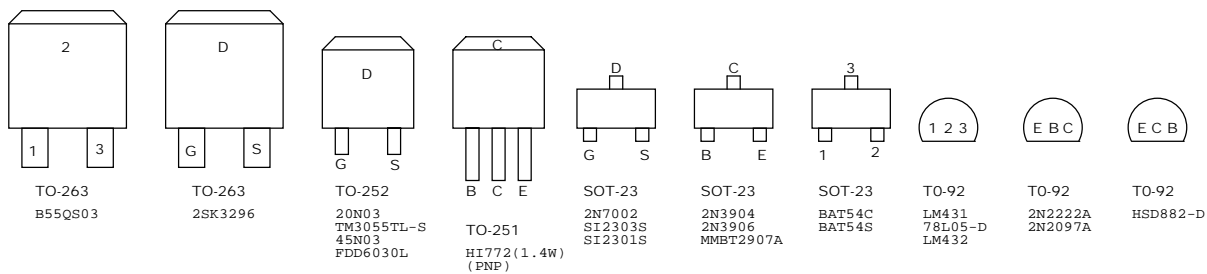
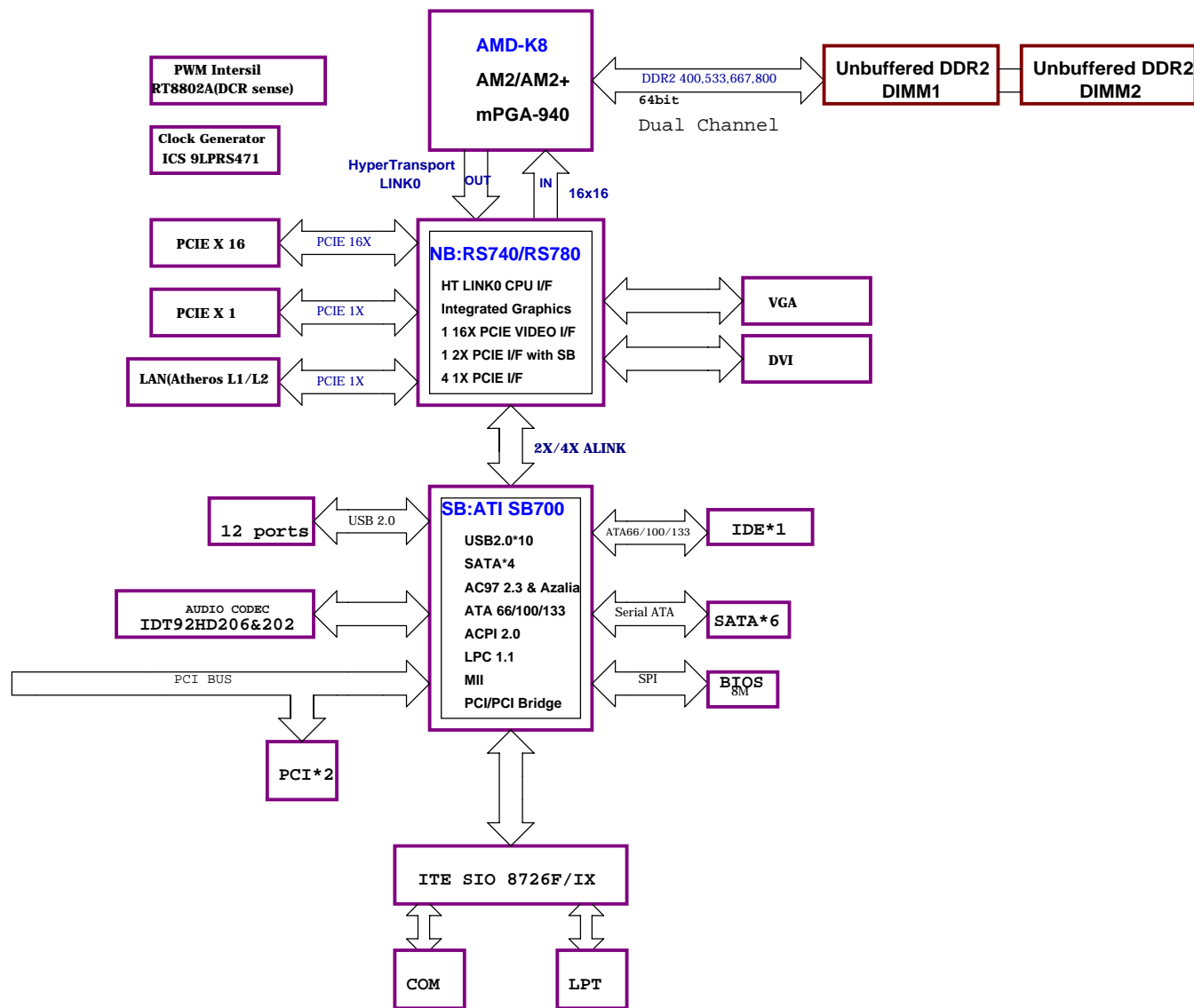


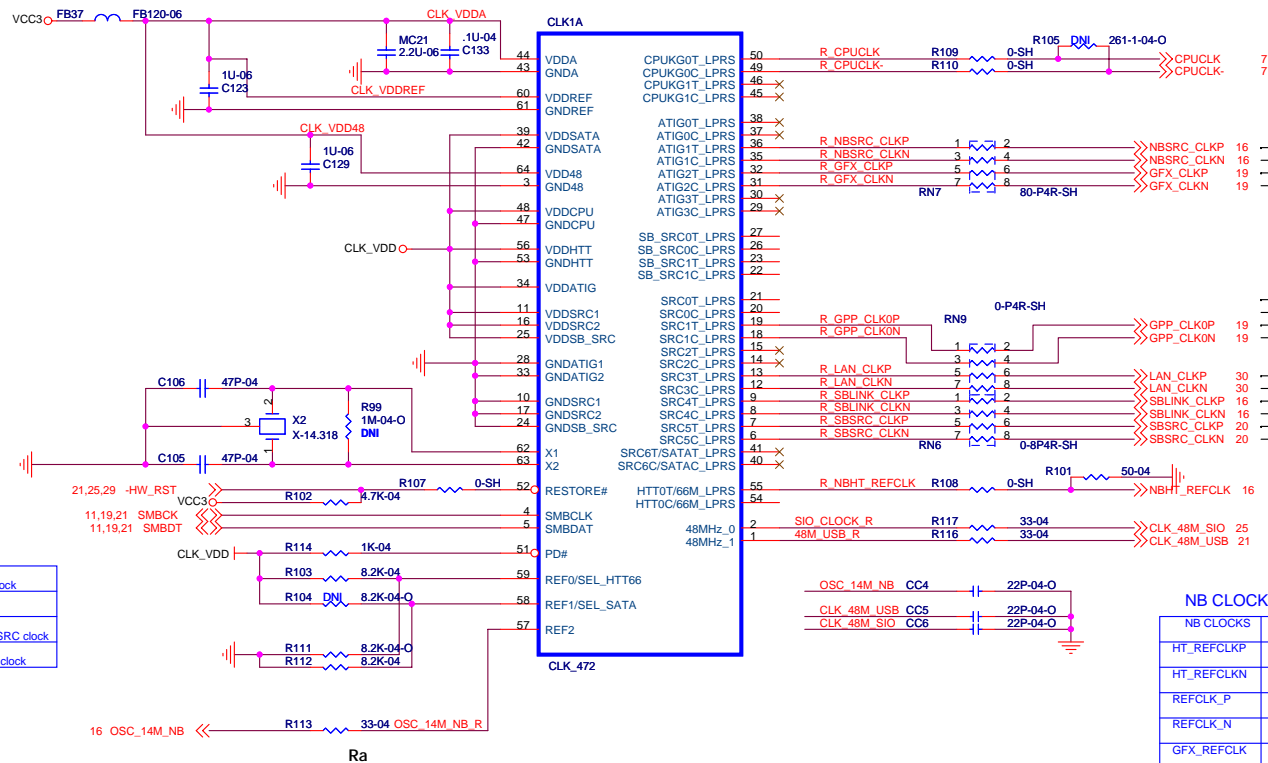
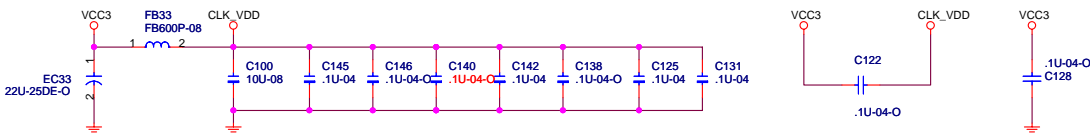
3) DESIGN NOTES in red are critical, and must be understood and followed.

@ ECS CONFIDENTIAL @

PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

		Elitegroup Computer Systems	
Title			
Cover Page			
Size	Document Number	Rev	
Custom	RS740M-M	1.0	
Date:	Monday, December 10, 2007	Sheet	1 of 35

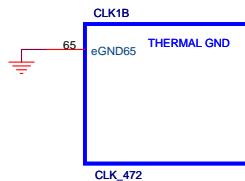




SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock

* default

Table1	RS740	RX780	RS780
OSC_14M_NB Voltage Leve	3.3V	1.8V	1.1V
Ra	33 OHM	75 OHM	200 OHM
Rb	NC	100 OHM	100 OHM



□ NB PCI-E GFX CLK
□ For GFX SLOT

□ For RX780 Only
□ For PCI-E 1X SLOT

□ For LAN CHIP
□ For A-Link(NB)
□ For A-Link(SB)

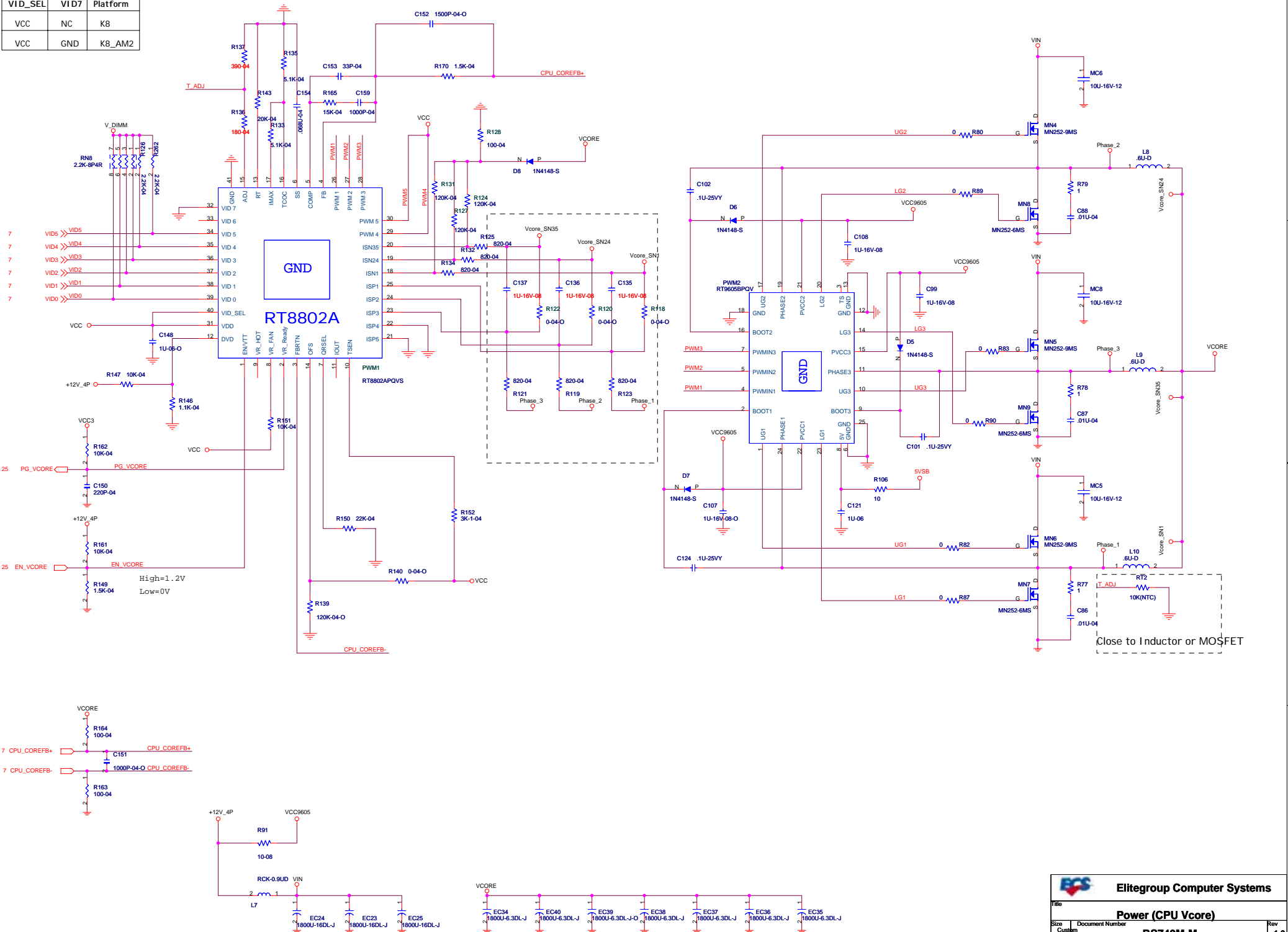
□ HT REF CLK

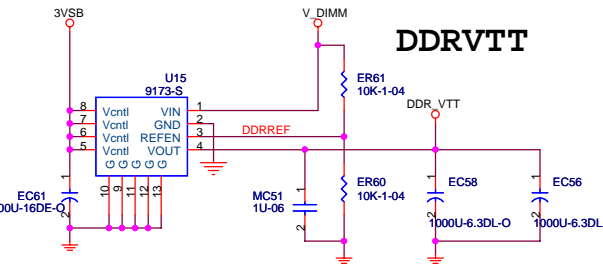
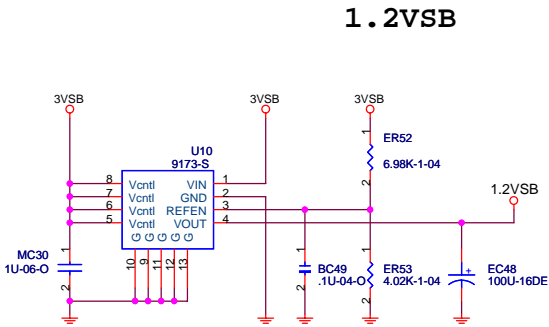
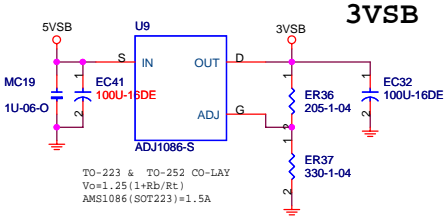
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF	R892
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	OSC_14M_NB
REFCLK_N	NC	NC	vref	
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	NBGPP_CLKP/N
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

VID_SEL	VID7	Platform
VCC	NC	K8
VCC	GND	K8_AM2

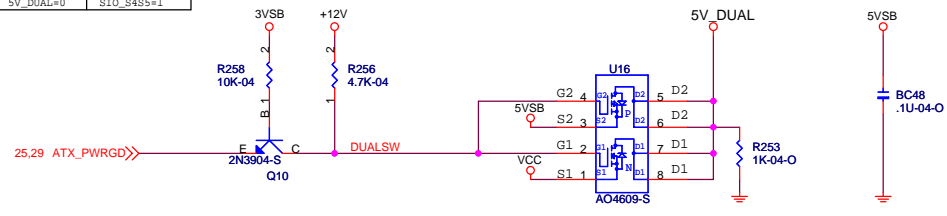




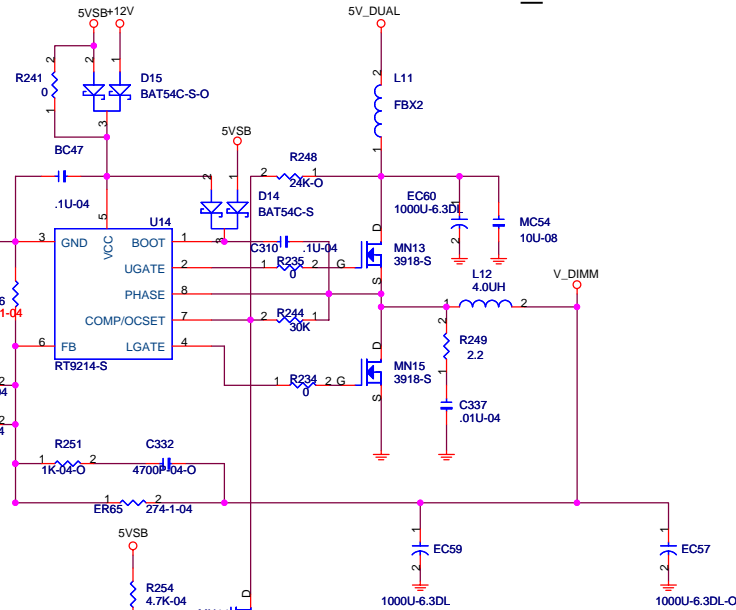
SIO_GP20	SIO_GP21	V_DIMM
1	1	Normal
0	1	+50mV
1	0	+100mV
0	0	+150mV



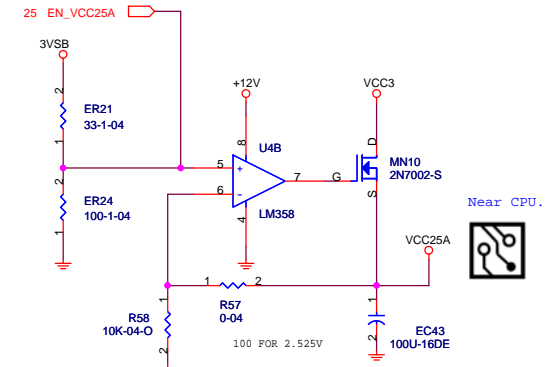
Status	Target	Super I/O P/GXS
AC plug	5V_DUAL=0	SIO_S4S5=0.D=1
S0,S1	5V_DUAL=VCC	SIO_S4S5=1
S3	5V_DUAL=5VSB	SIO_S4S5=0
S4,S5	5V_DUAL=5VSB	SIO_S4S5=0
S4,S5	5V_DUAL=0	SIO_S4S5=1



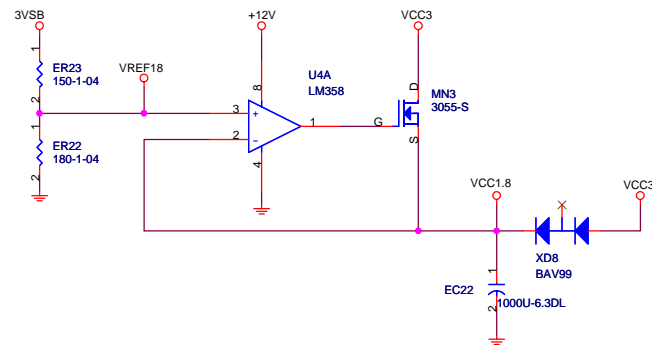
V_DIMM



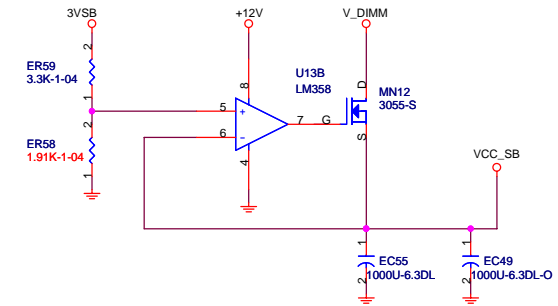
VCC25A



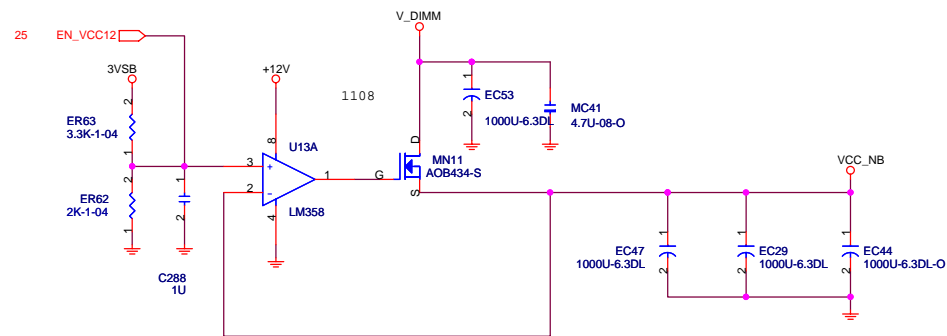
VCC1.8



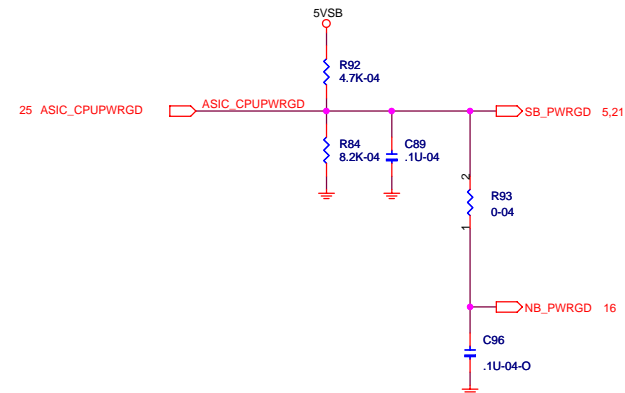
VCC_SB



VCC_NB & VCC1.2



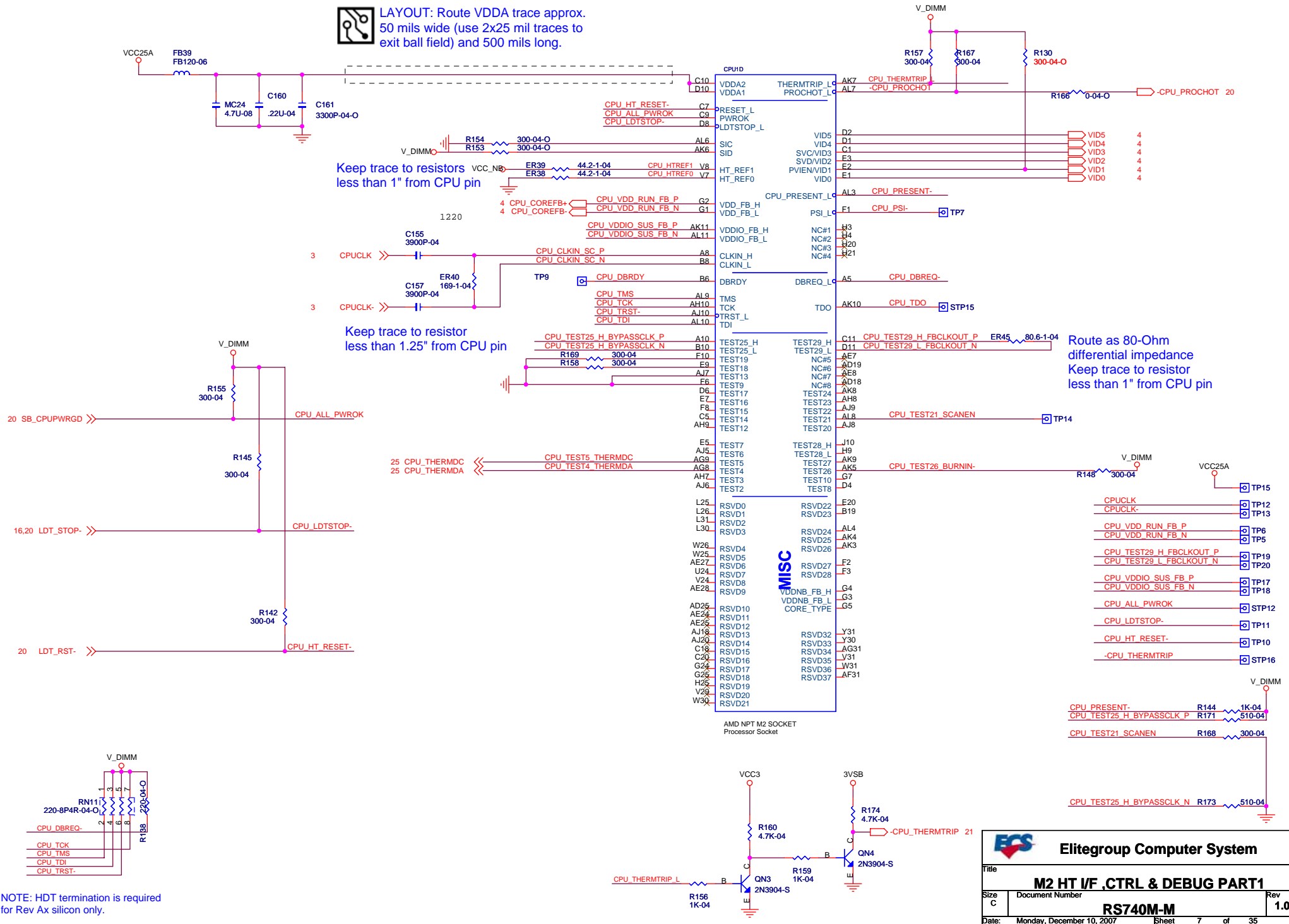
SB&NB PWRGOOD



ATHLON Control and Debug

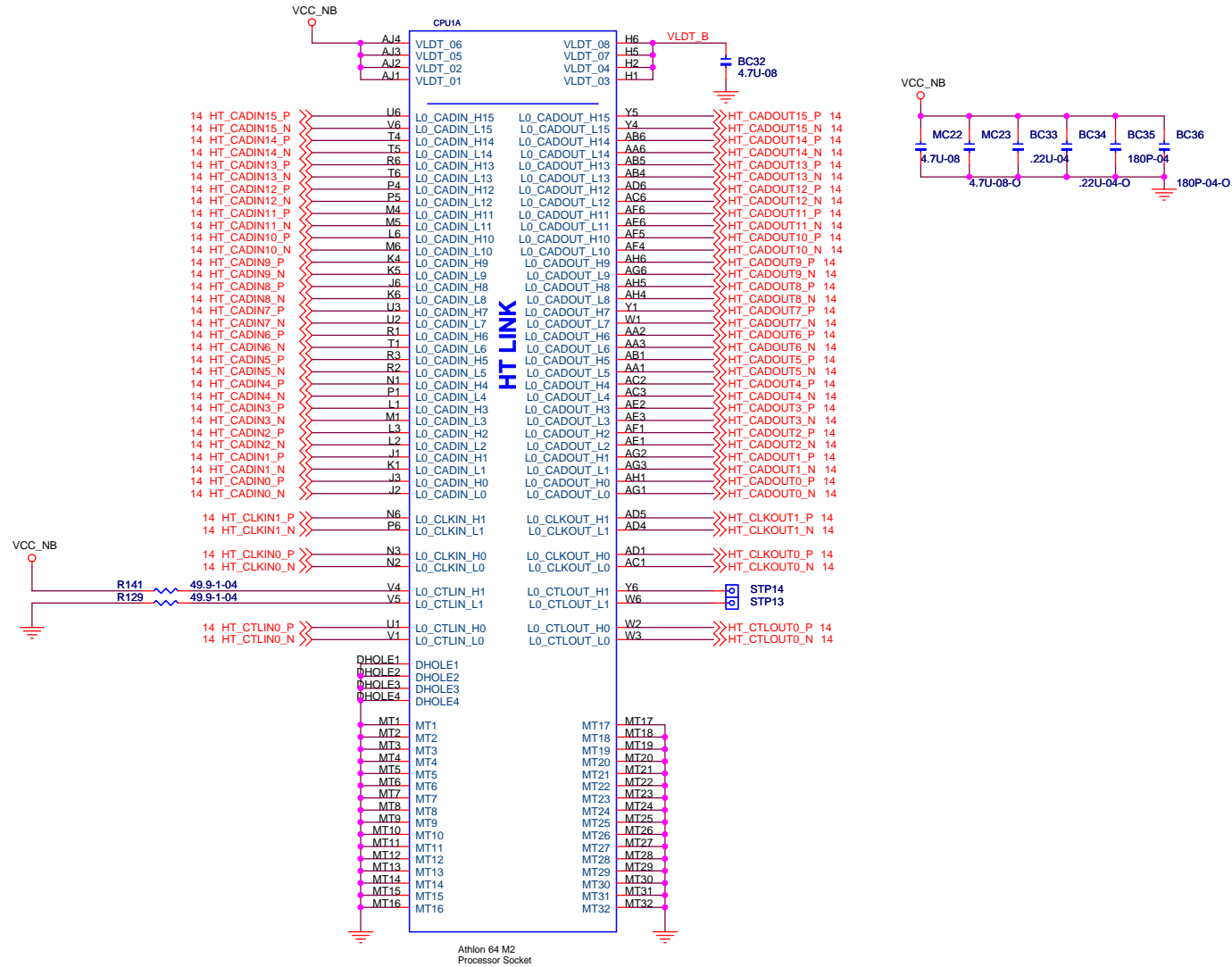


LAYOUT: Route VDDA trace approx.
50 mils wide (use 2x25 mil traces to
exit ball field) and 500 mils long.



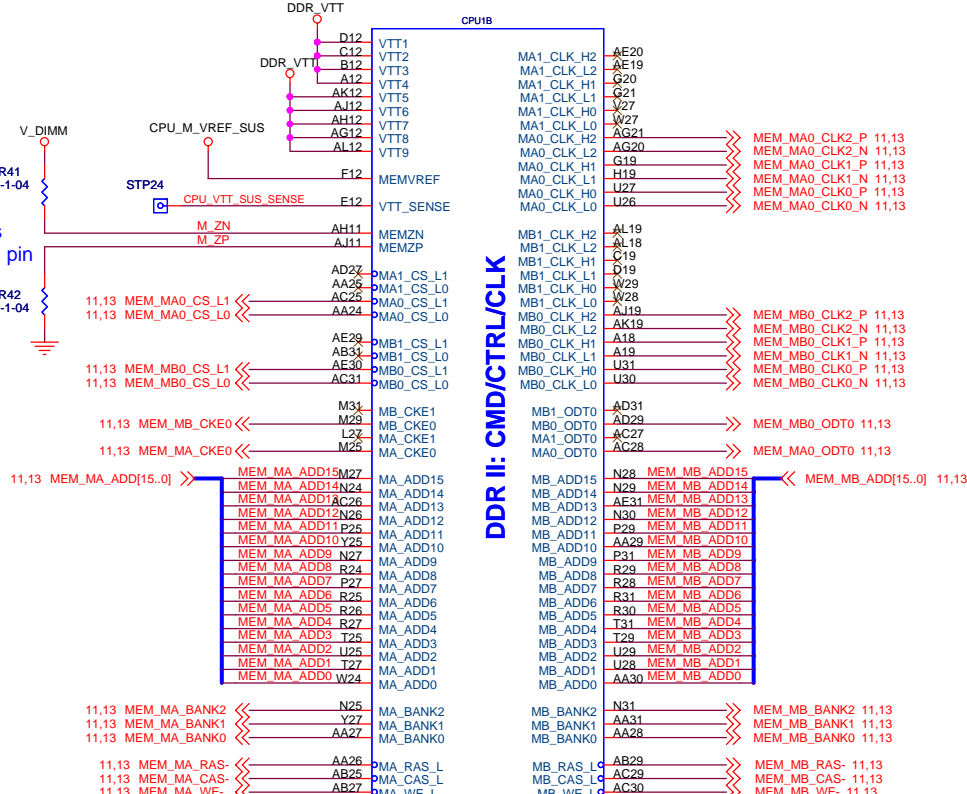
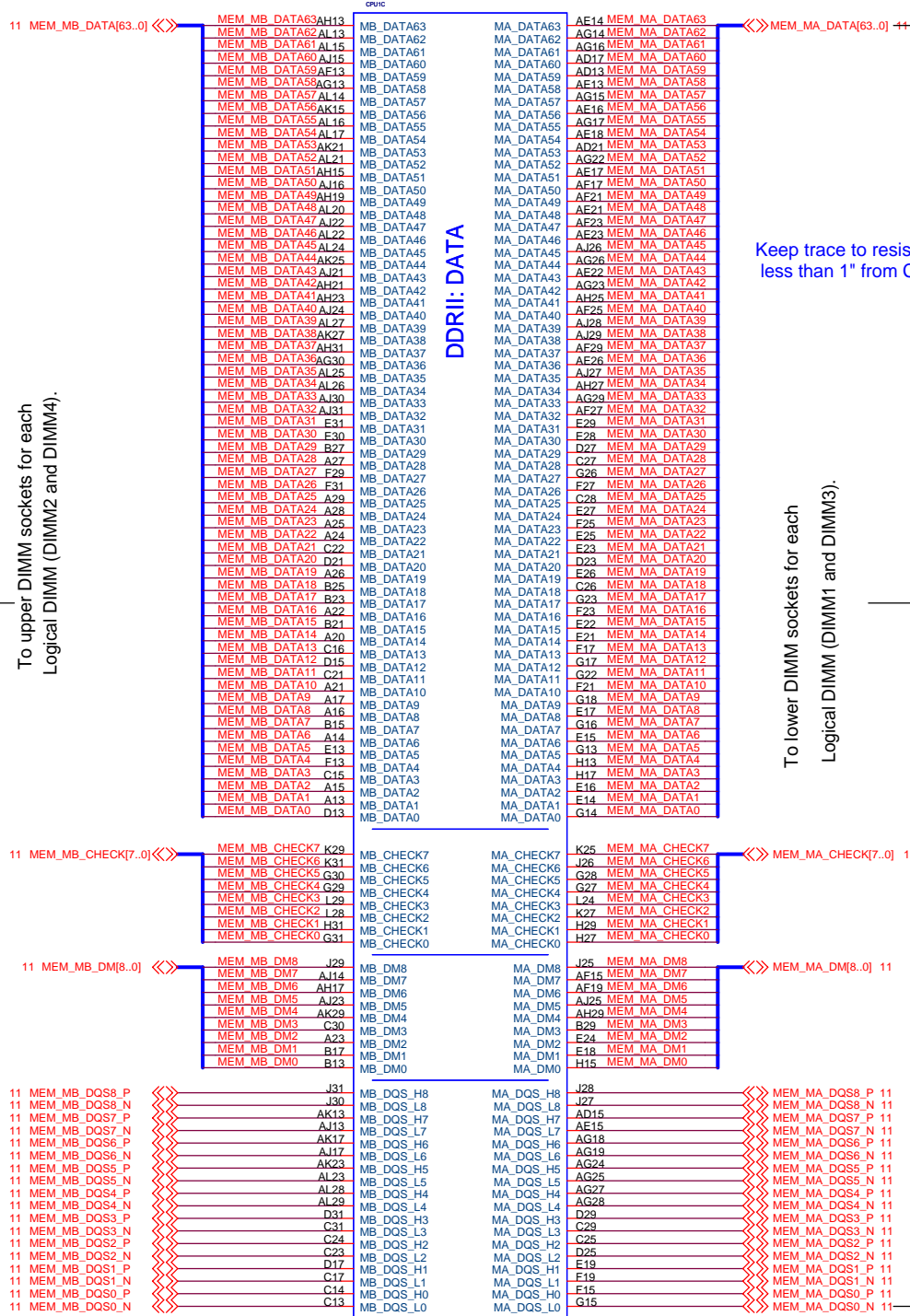
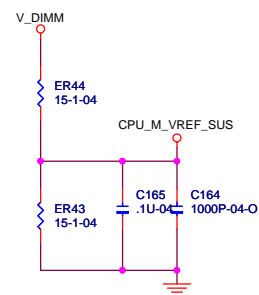
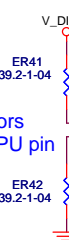
CPU HyperTransport Interface

VDDLDRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

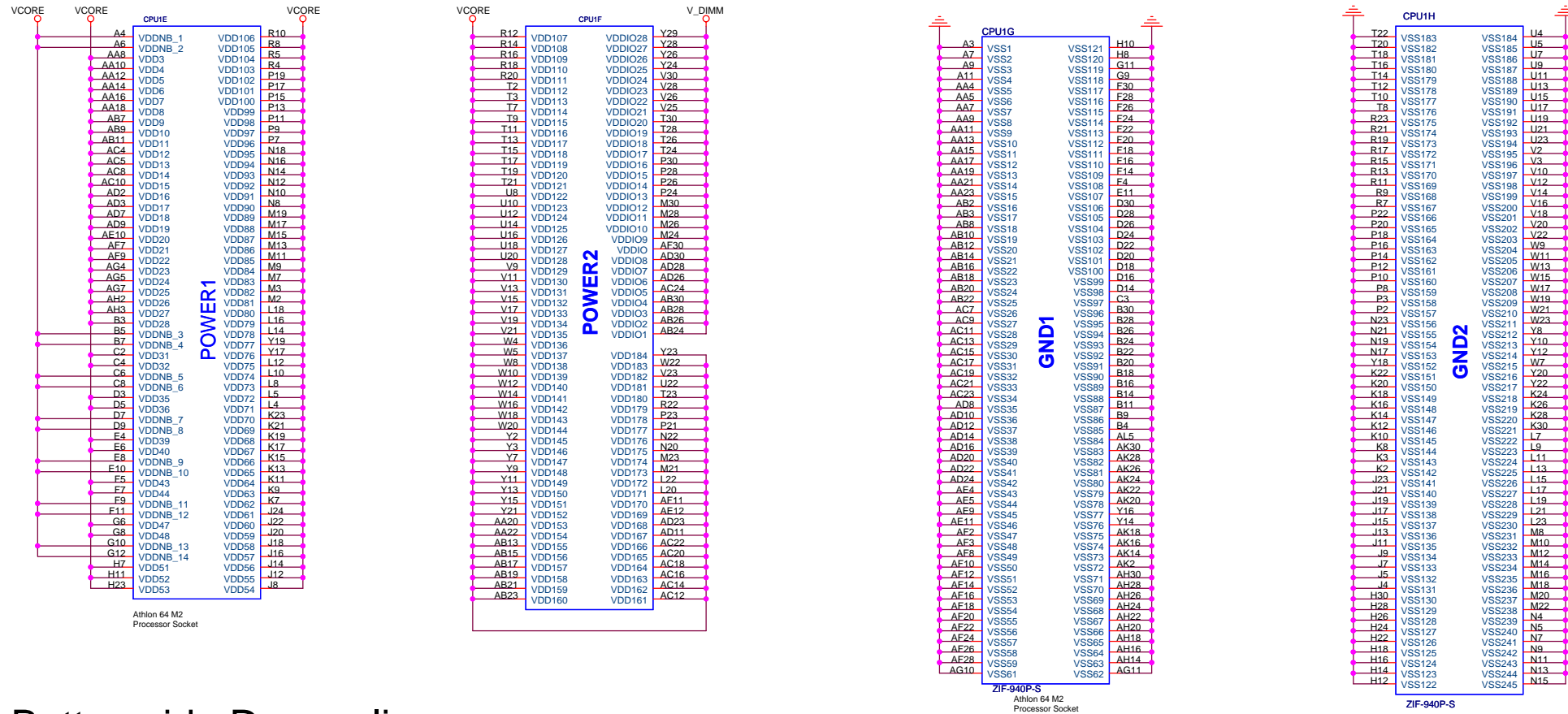




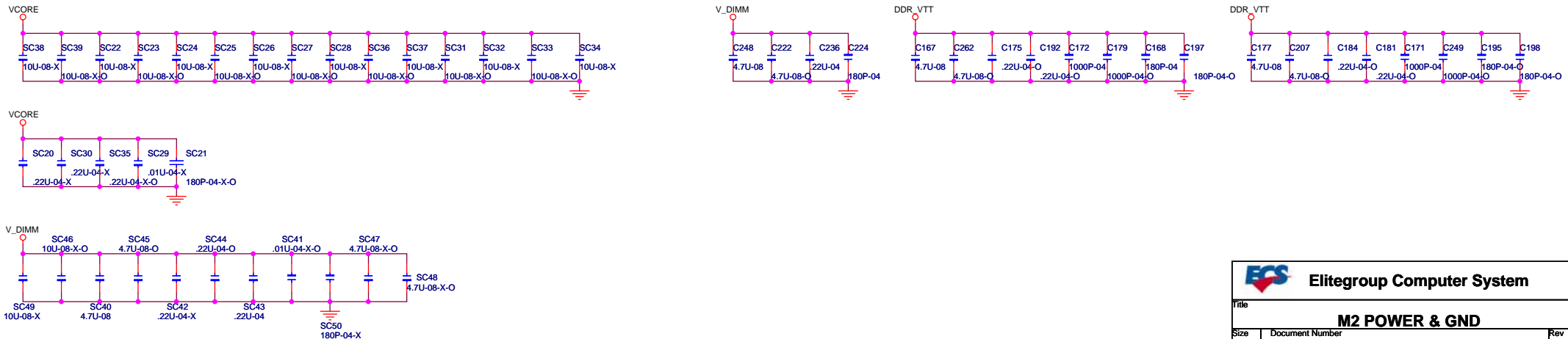
Keep trace to resistors
less than 1" from CPU



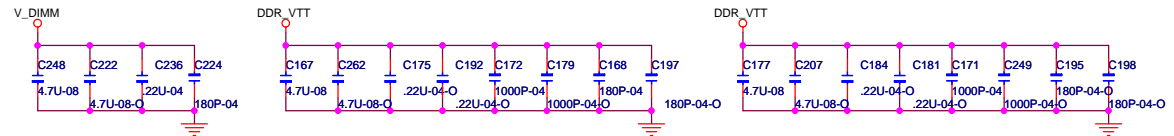
Processor Power and Ground

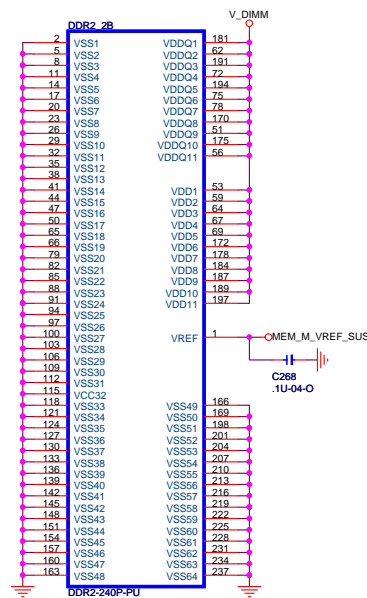
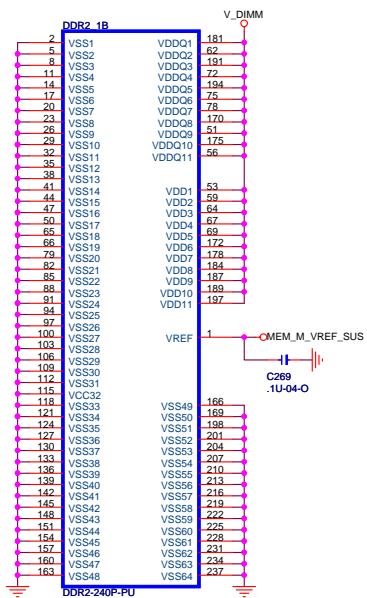


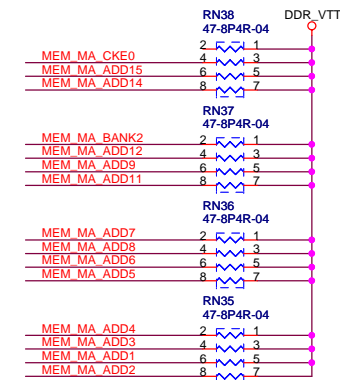
Bottomside Decoupling



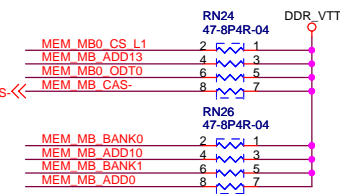
Decoupling between processor and DIMMs
Place as close to processor as possible



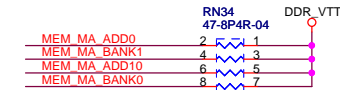




9,11 MEM_MA_ADD[15..0] << MEM_MA_ADD[15..0]



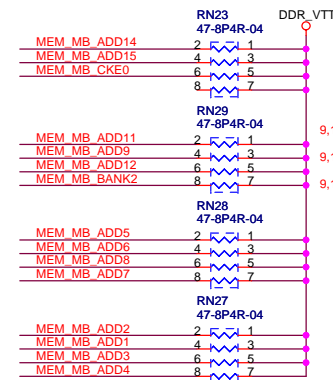
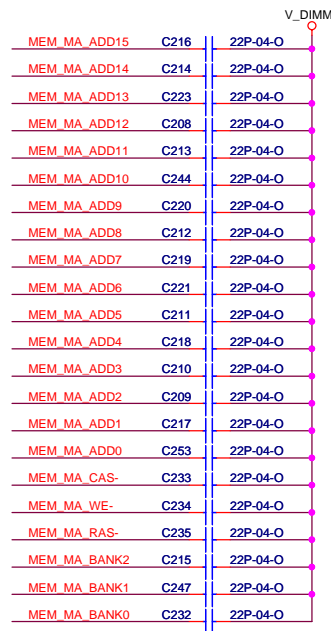
9,11 MEM_MA_BANK[2..0] << MEM_MA_BANK[2..0]



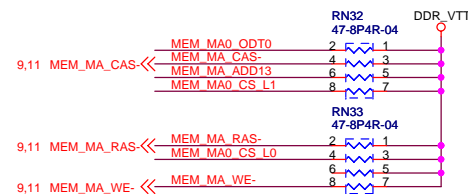
9,11 MEM_MA_CKE0 << MEM_MA_CKE0
9,11 MEM_MA0_ODT0 << MEM_MA0_ODT0

9,11 MEM_MA0_CS_L[1..0] << MEM_MA0_CS_L[1..0]

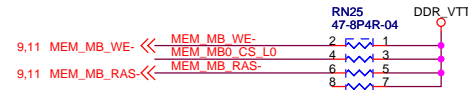
9,11 MEM_MA0_CLK2_P << C196 | 1.5P-04-O >> MEM_MA0_CLK2_N 9,11
9,11 MEM_MA0_CLK1_P << C191 | 1.5P-04-O >> MEM_MA0_CLK1_N 9,11
9,11 MEM_MA0_CLK0_P << C204 | 1.5P-04-O >> MEM_MA0_CLK0_N 9,11



9,11 MEM_MB_ADD[15..0] << MEM_MB_ADD[15..0]

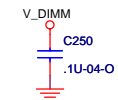
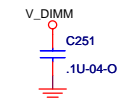
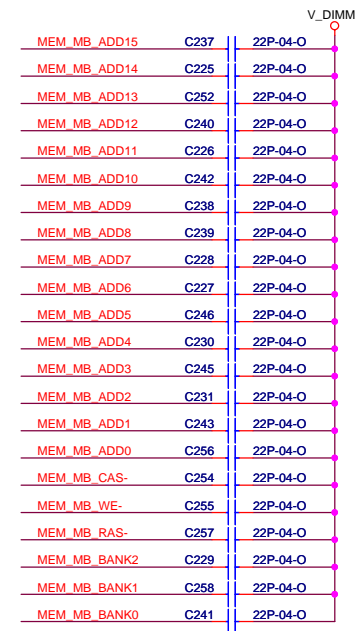


9,11 MEM_MB_BANK[2..0] << MEM_MB_BANK[2..0]



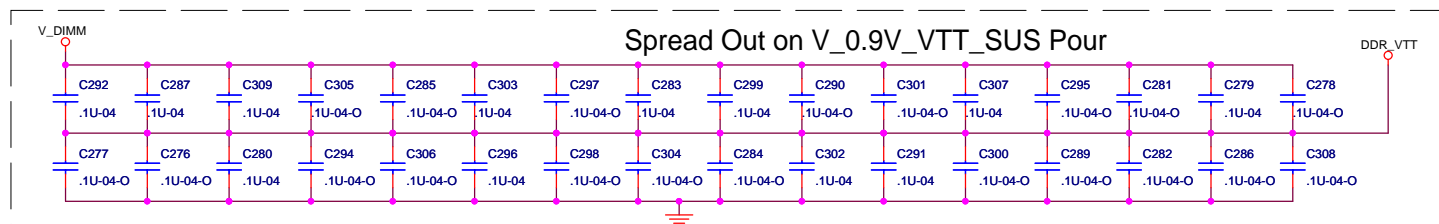
9,11 MEM_MB_CKE0 << MEM_MB_CKE0
9,11 MEM_MB0_ODT0 << MEM_MB0_ODT0

9,11 MEM_MB0_CS_L[1..0] << MEM_MB0_CS_L[1..0]

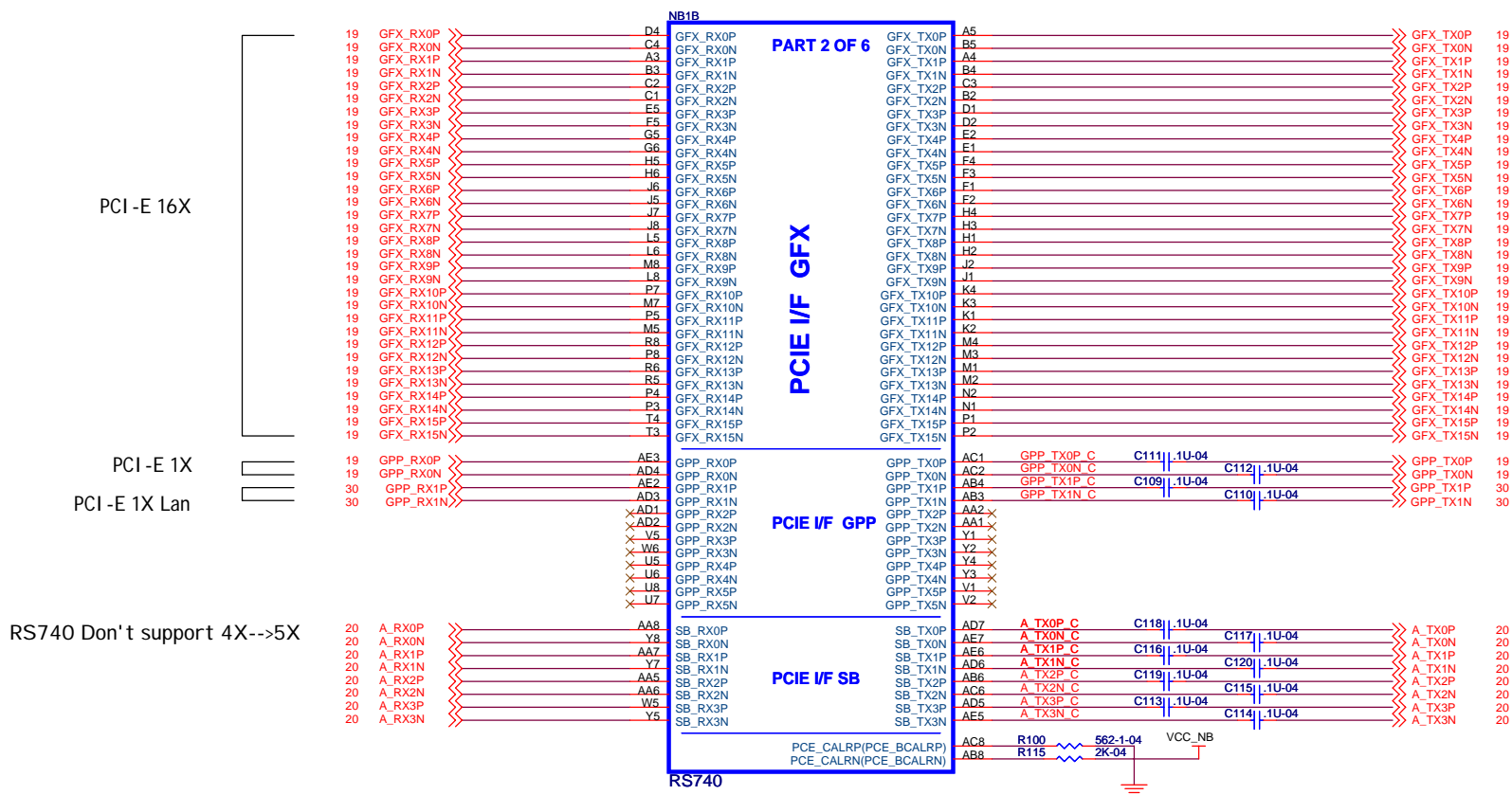


Place one capacitor between two resistor array

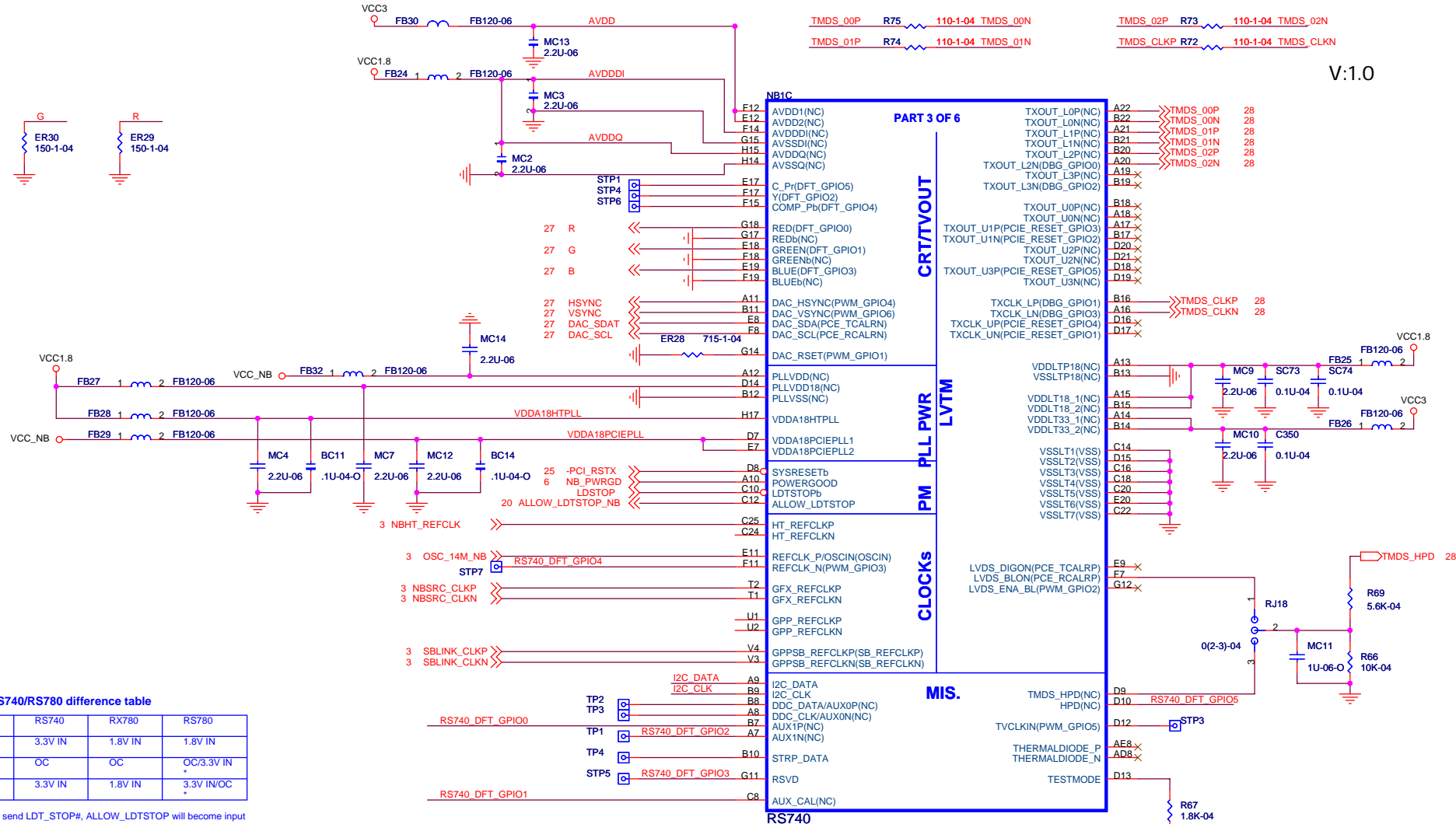
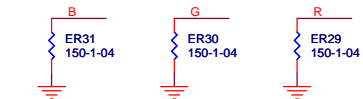
Spread Out on V_0.9V_VTT_SUS Pour







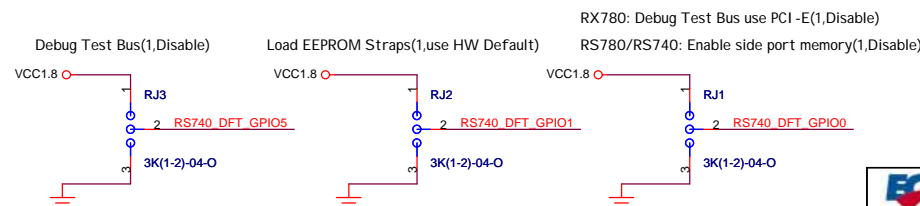
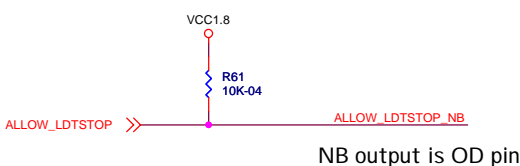
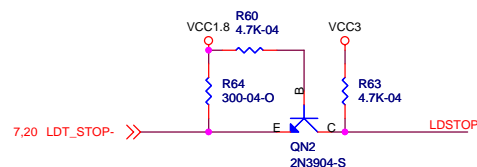
V:1.0



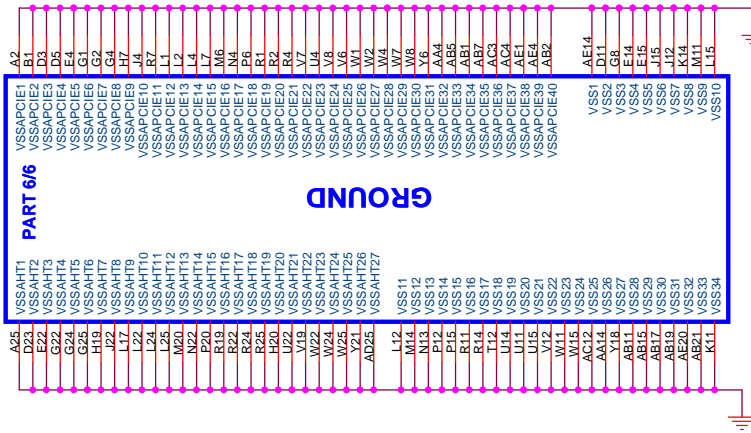
RX740/RS740/RS780 difference table

	RS740	RX780	RS780
NB_PWRGD_IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP_OUT(default)/IN	OC	OC	OC/3.3V IN
LDT_STOP#_IN(default)/IN	3.3V IN	1.8V IN	3.3V IN/OC

*. CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

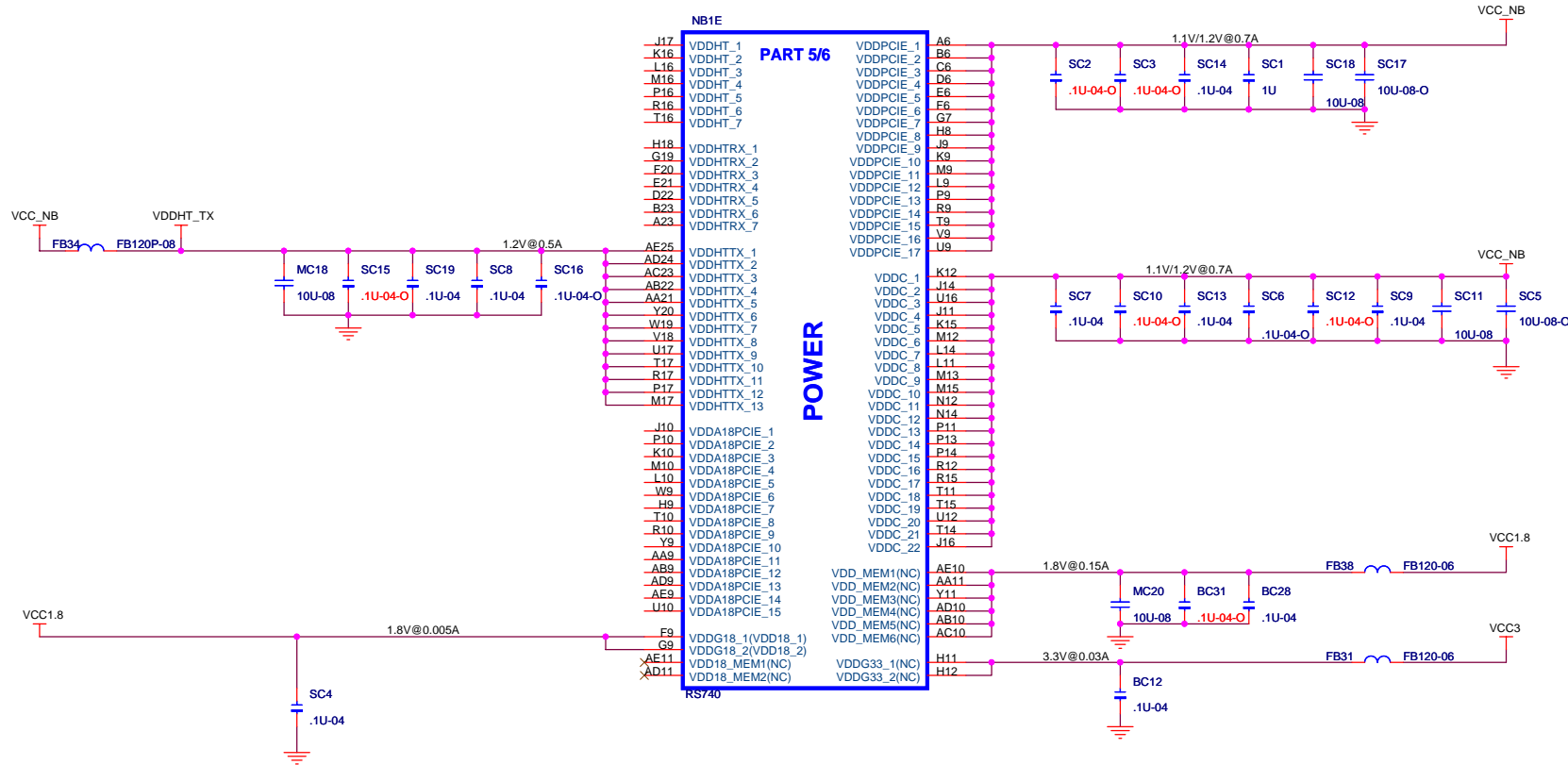


NB1F
RS740



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLTP18	+1.8V	NC	+1.8V



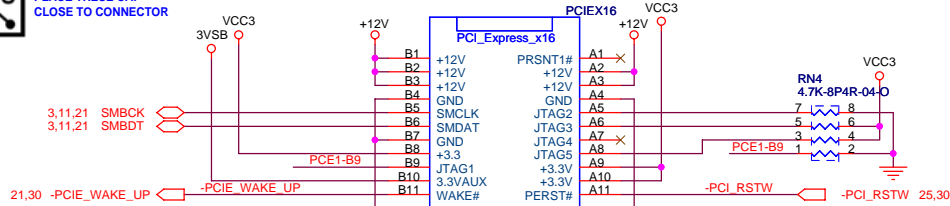
PCI_EXPRESS_x16

+12V : 5, 5Amp

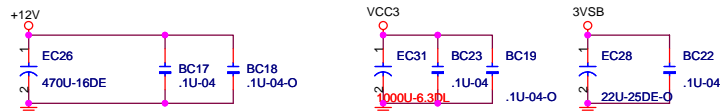
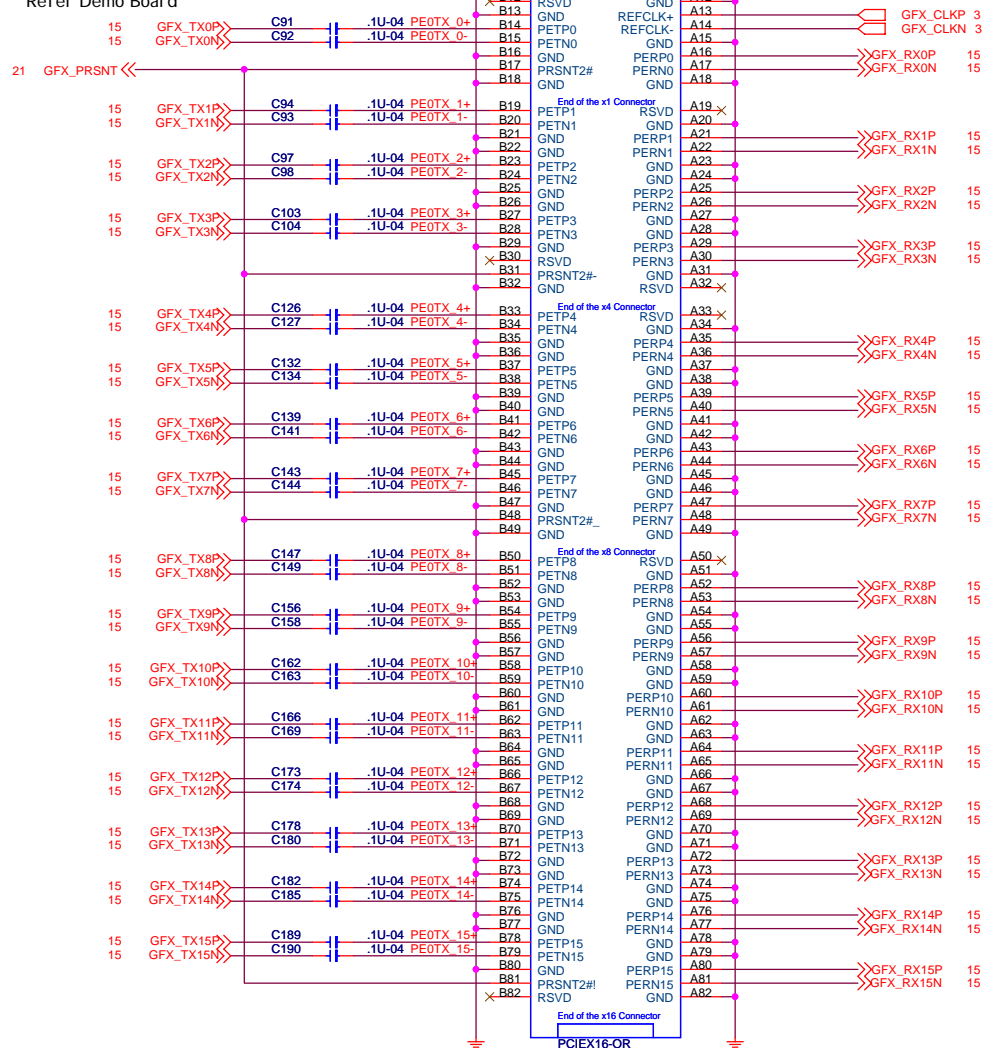
Color:Orange



PLACE THESE CAP
CLOSE TO CONNECTOR



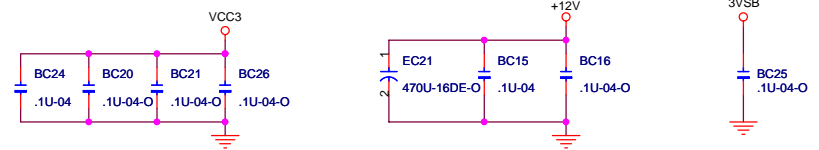
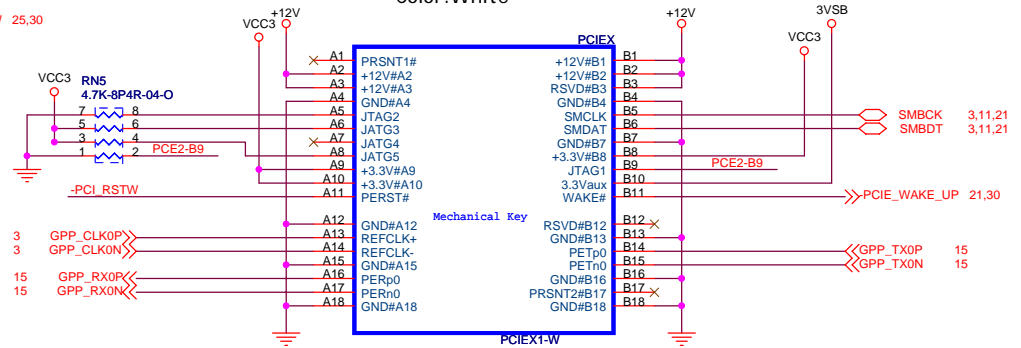
Refer Demo Board



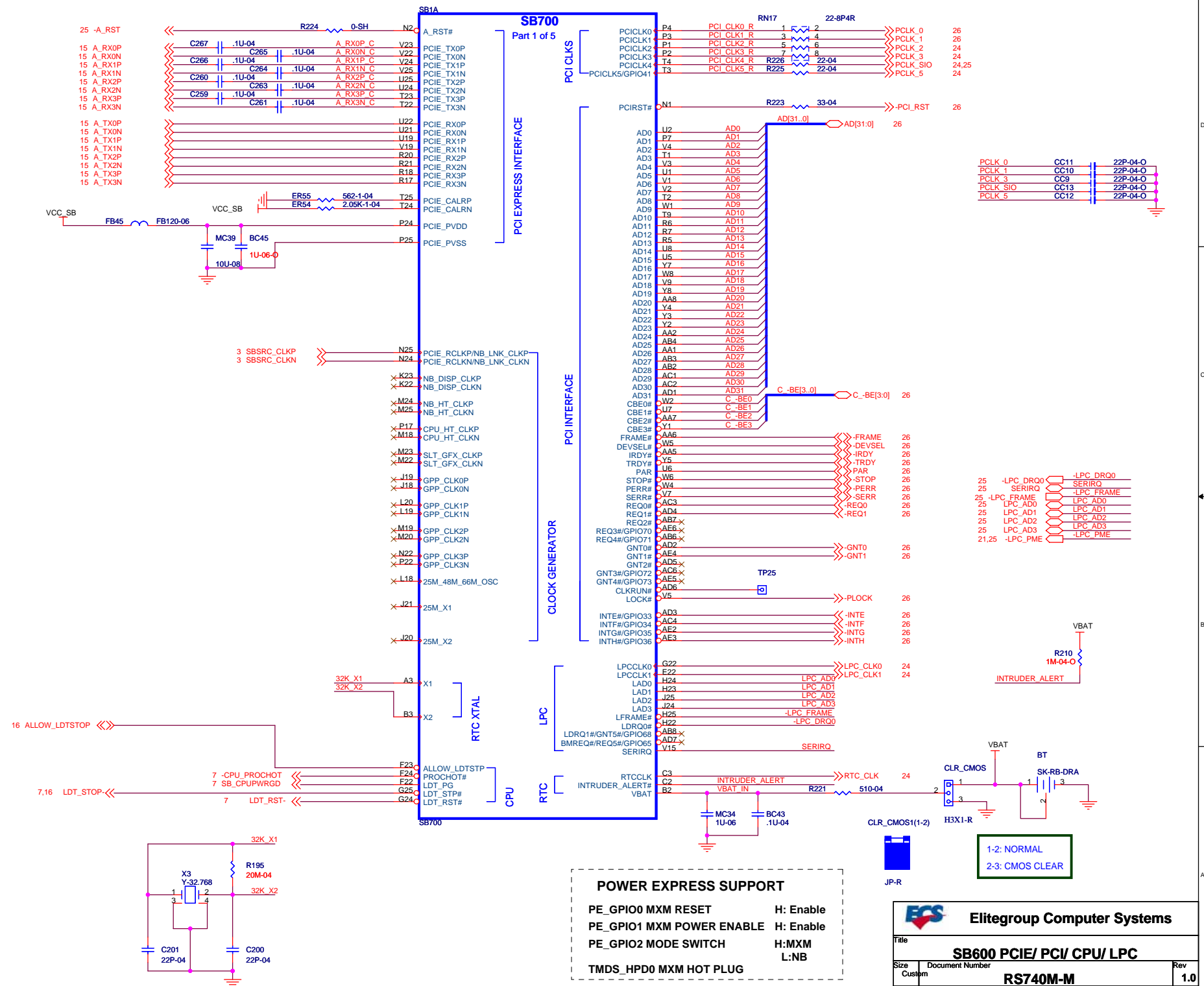
V1.0

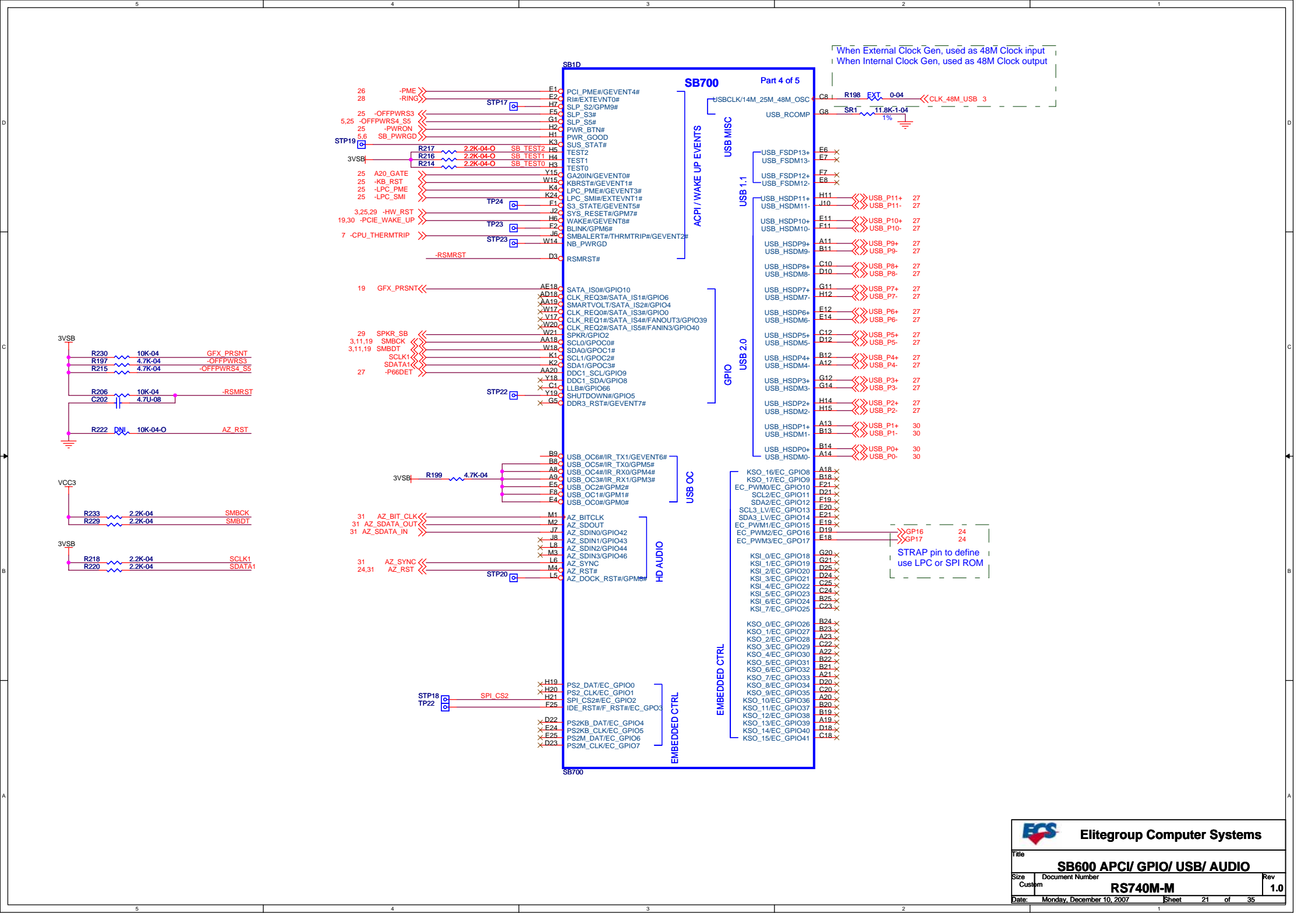
PCI_EXPRESS_x1

Color:White

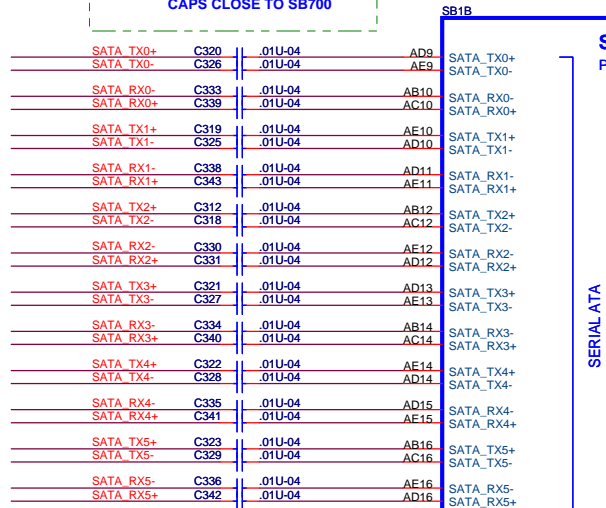


Title			
PCI EXPRESS x16 SLOTS			
Size	Document Number	Rev	
C	RS740M-M	B	
Date:	Monday, December 10, 2007	Sheet	19 of 35



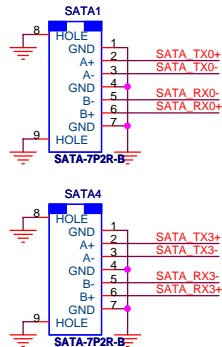
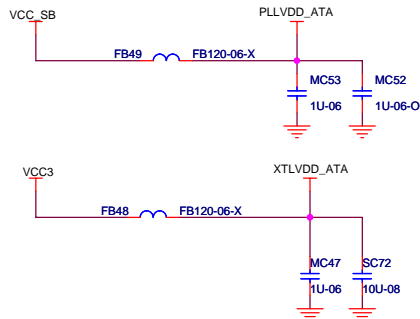
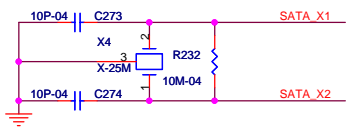


PLACE SATA AC COUPLING
CAPS CLOSE TO SB700



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB700

NOTE:
SR2 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

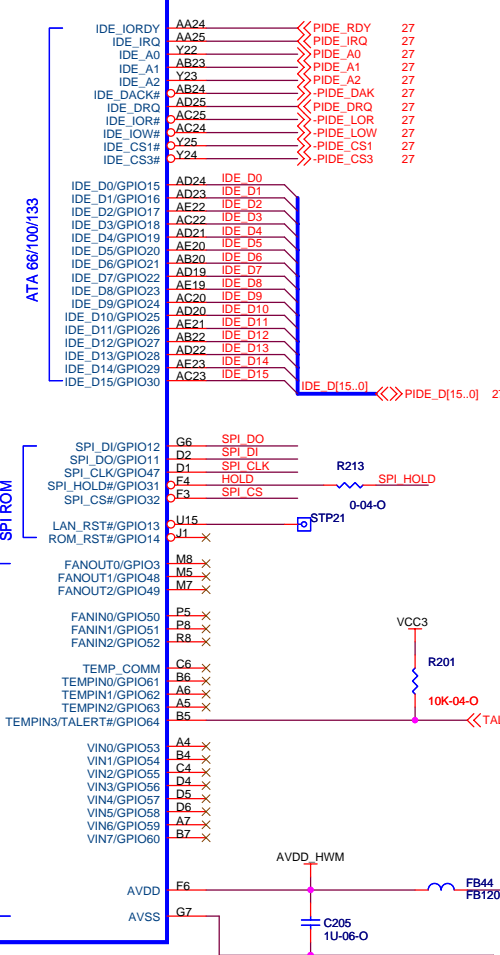


SB700
Part 2 of 5

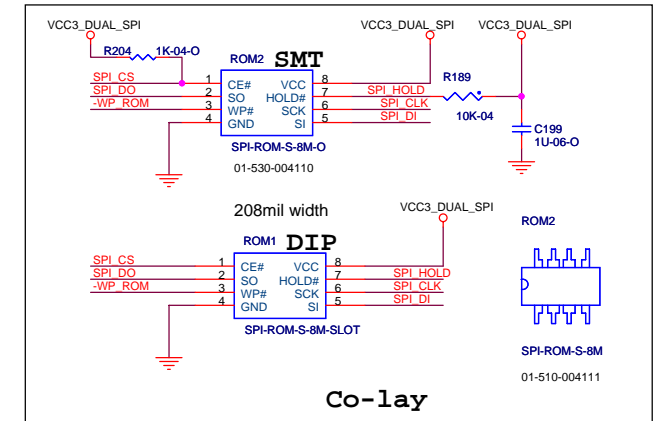
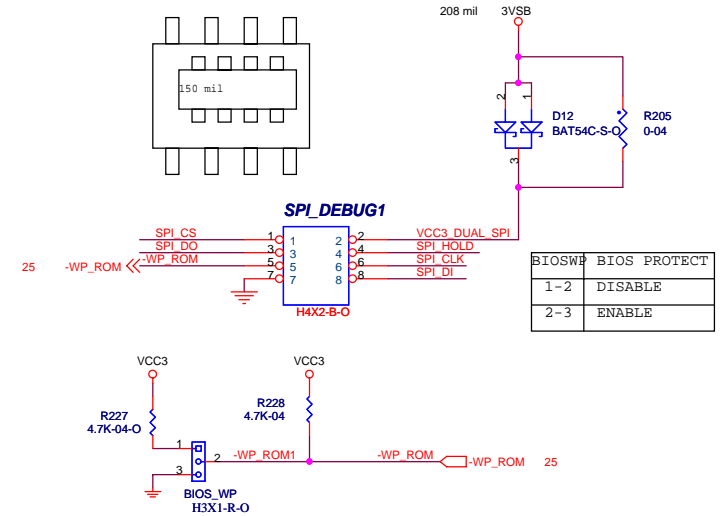
SERIAL ATA

SPI ROM

HW MONITOR



SO8 MN and MW co-layout layout draw

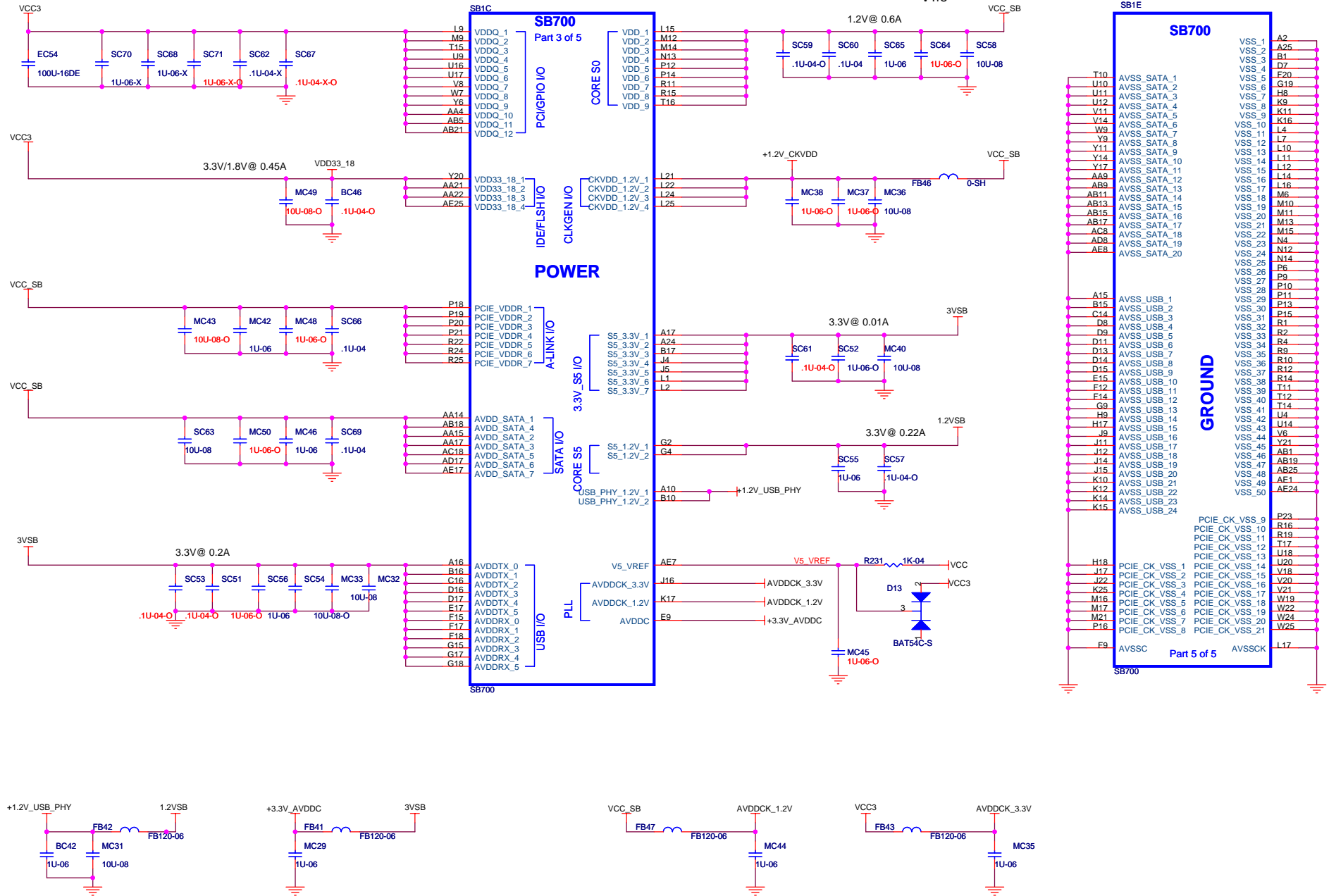


for SPI ROM

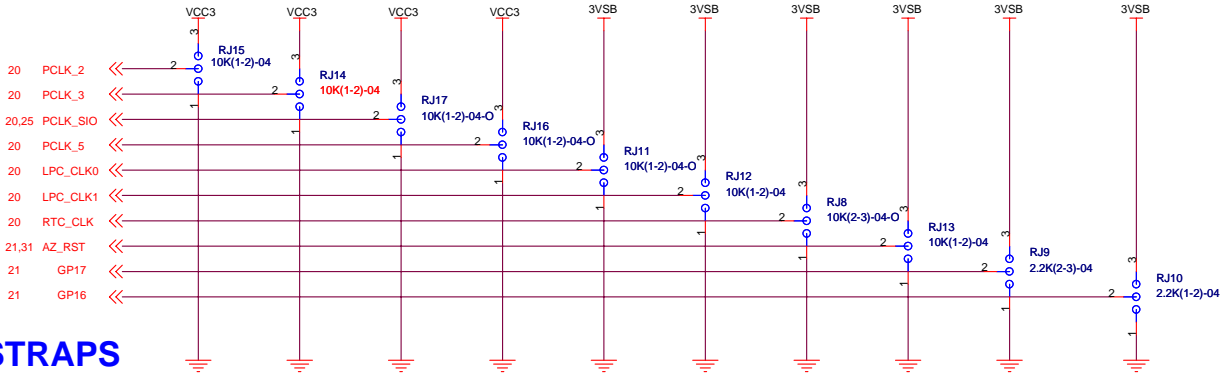
HWM_AGND TRACE AT LEAST
10MIL WIDE

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

V1.0



NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

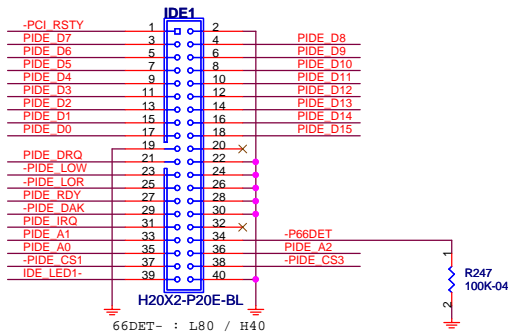
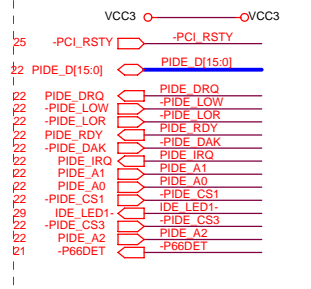
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	Watchdog ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC Enable	CLKGEN ENABLED	INTERNAL RTC	PCI ROM BOOT Enable	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	Watchdog DISABLED	IGNORE DEBUG STRAPS			IMC Disable	CLKGEN DISABLED	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	PCI ROM BOOT Disable	L, H = LPC ROM	L, L = FWH ROM

A12

A12

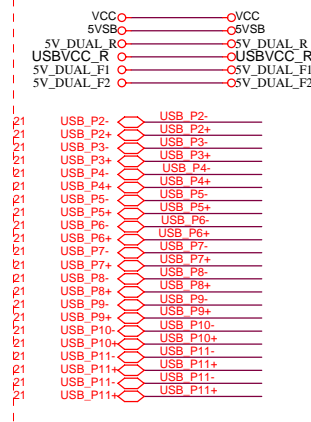
External Connection

2007/08/20

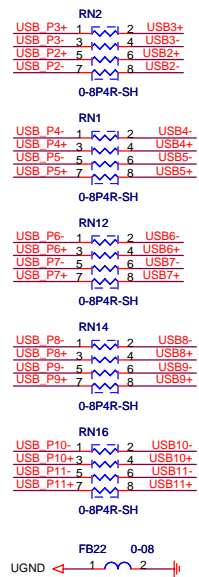


	ATi	Intel	NV	VIA	Sis
Pin 3	PDP7:	X	Pull Hi: 4.7K	Pull Hi: 4.7K	X
Pin 21	PDP8Q	X	Pull Hi: 8.2K	Pull Hi: 4.7K	X
Pin 27	PDP8Q	X	Pull Lo: 10K	Pull Lo: 10K	Pull Lo: 5.6K
Pin 31	PIDE_IRQ	X	Pull Lo: 5.6K	Pull Lo: 5.6K	X
Pin 34	P66DET	100K	27K	10K	20K

External Connection

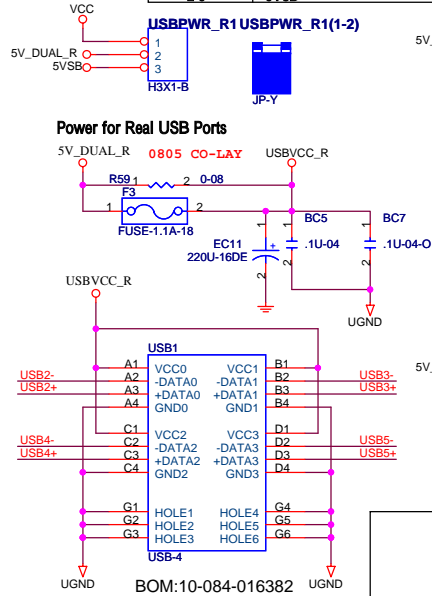


Change to Short Pad

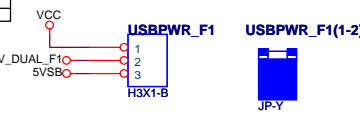


150 Mils Width

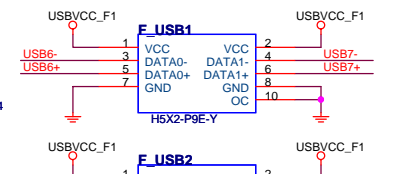
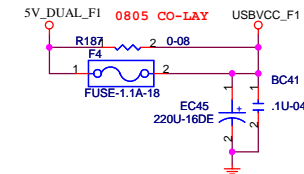
USBPWR_R1	USB POWER SELECT
1,2	VCC
2,3	5VSB



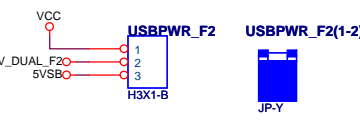
150 Mils Width



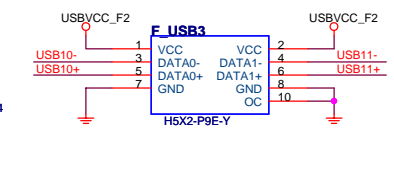
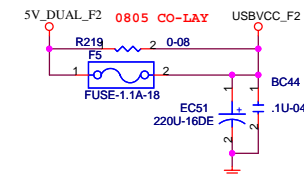
Power for Front USB Ports



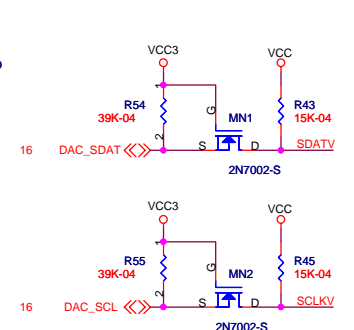
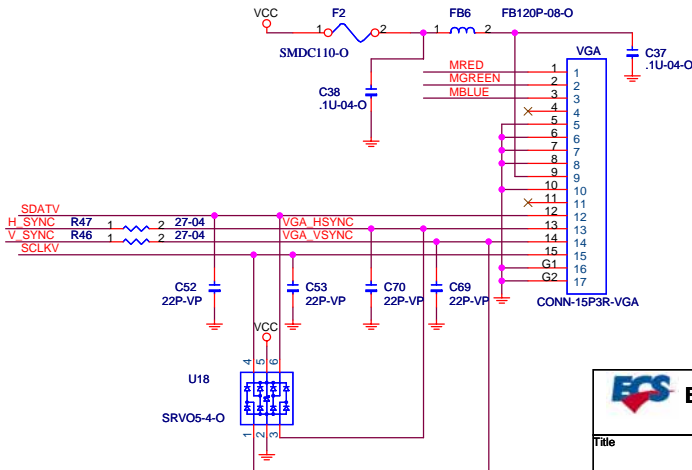
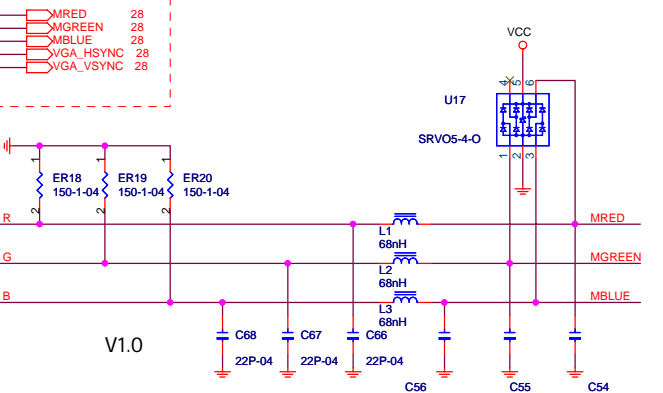
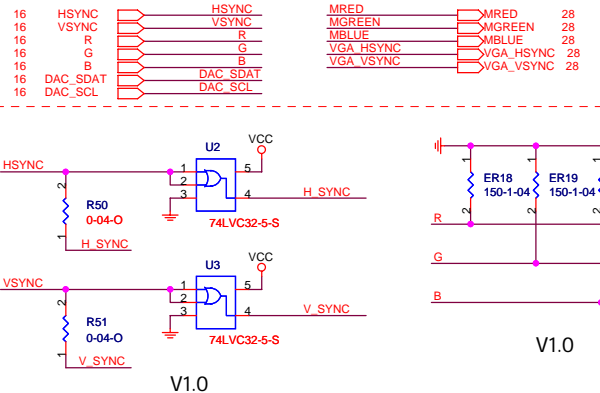
150 Mils Width



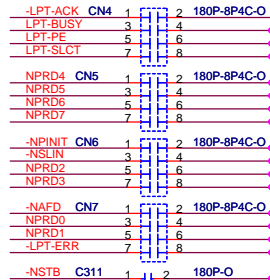
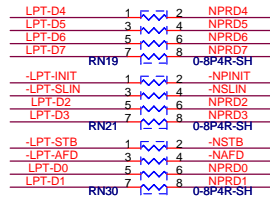
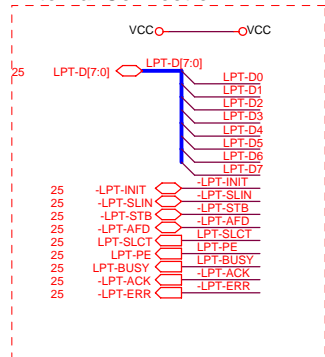
Power for Front USB Ports



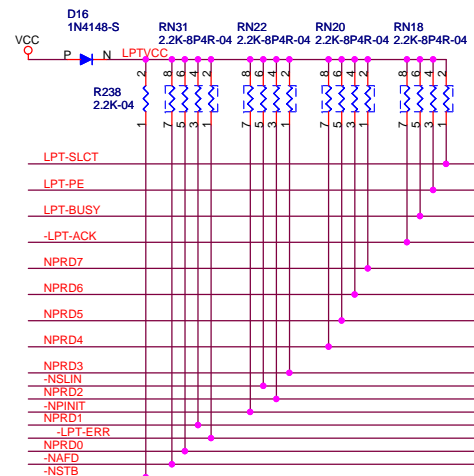
External Connection



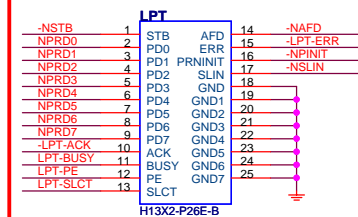
External Connection



BOM coherence

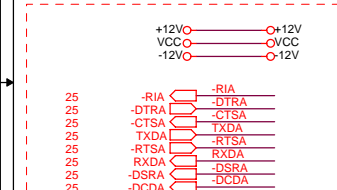


Selection design with LPT1



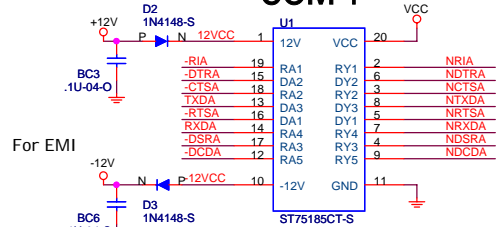
COM Ports

External Connection

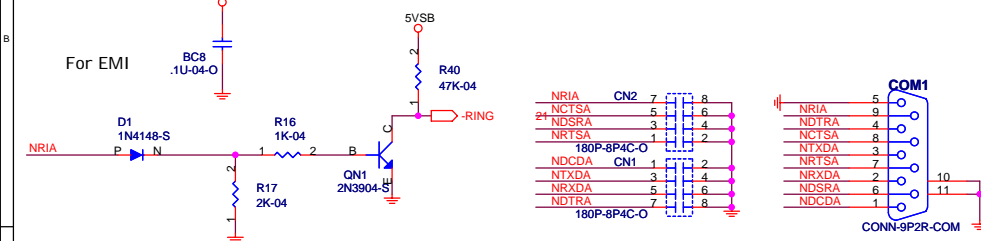


For EMI

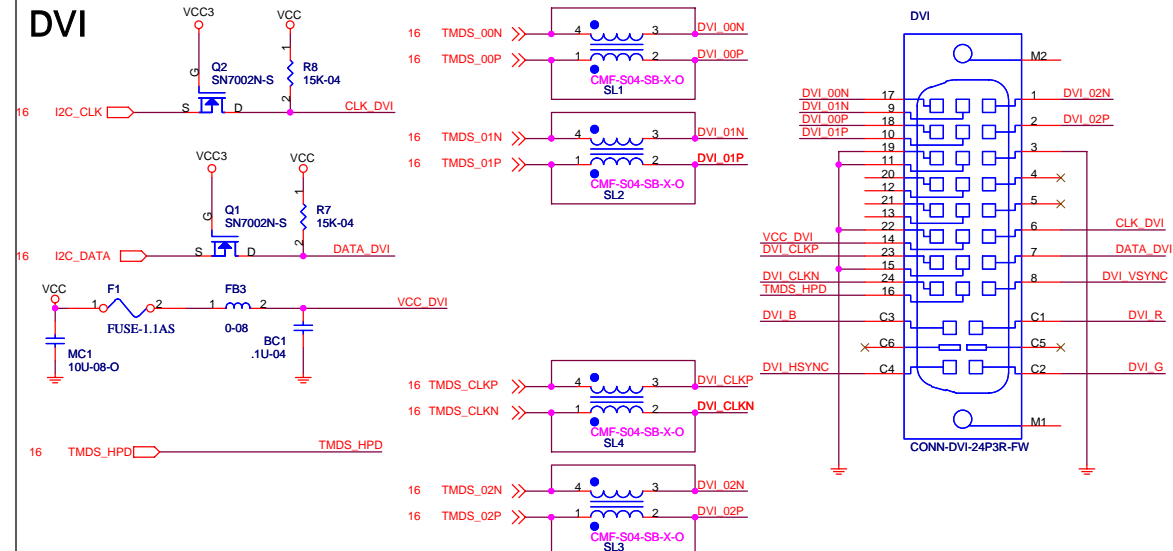
COM 1



For EMI

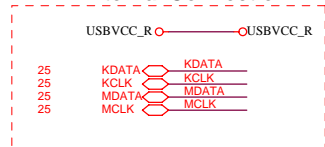


DVI

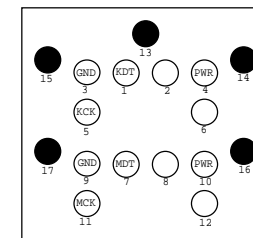
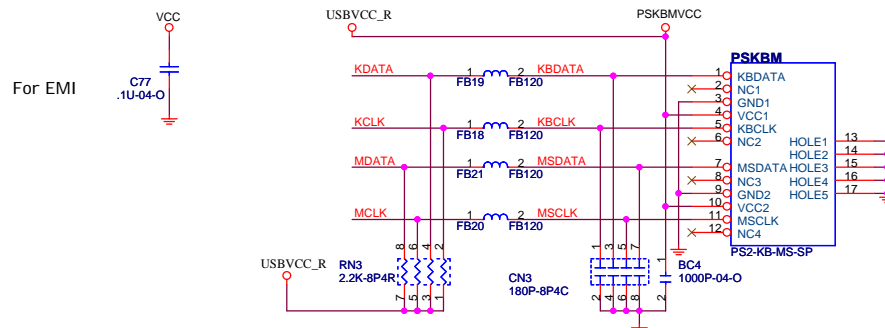


PSKBM

External Connection



For EMI



Elitegroup Computer Systems

LPT,COM,PSKBM,DVI

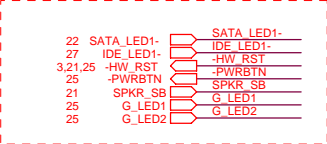
RS740M-M

Monday, December 10, 2007

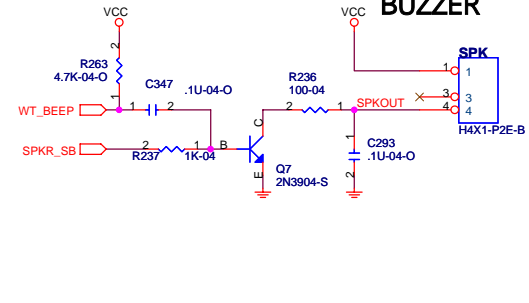
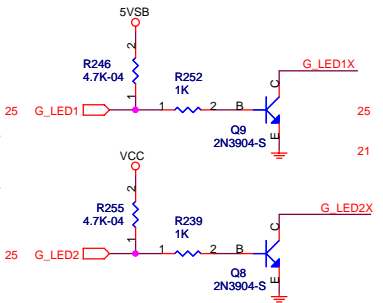
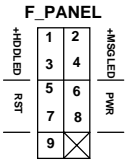
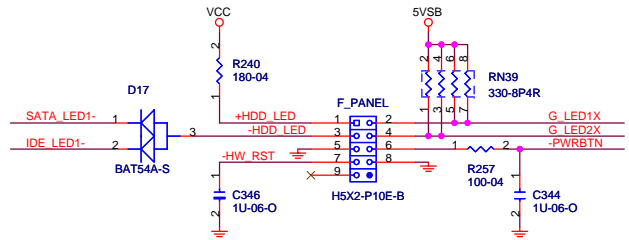
Sheet 28 of 35

FRONT PANEL

External Connection

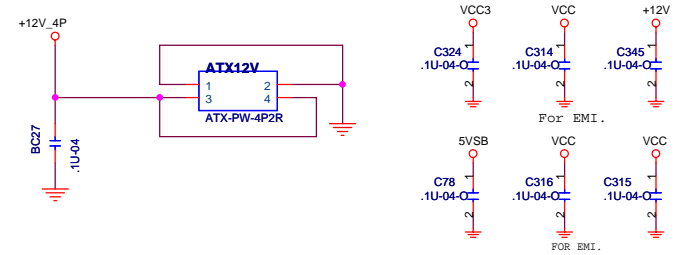
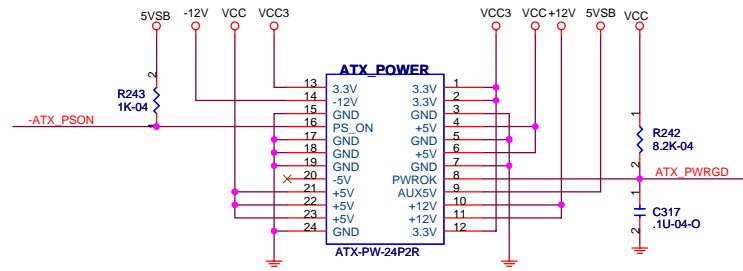
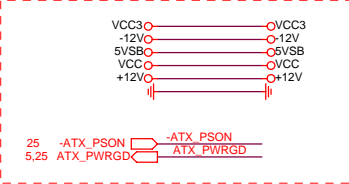


If you found anything wrong with this circuit, please contact with Jack Hu (Ext:622)



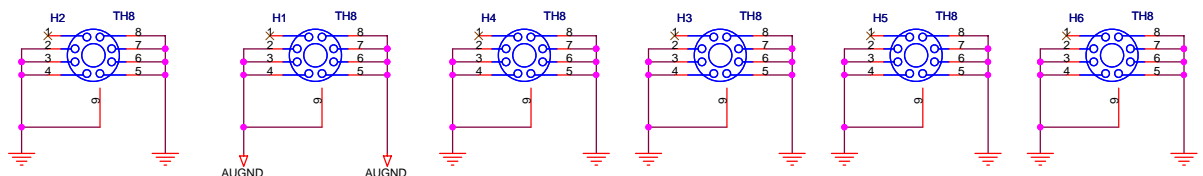
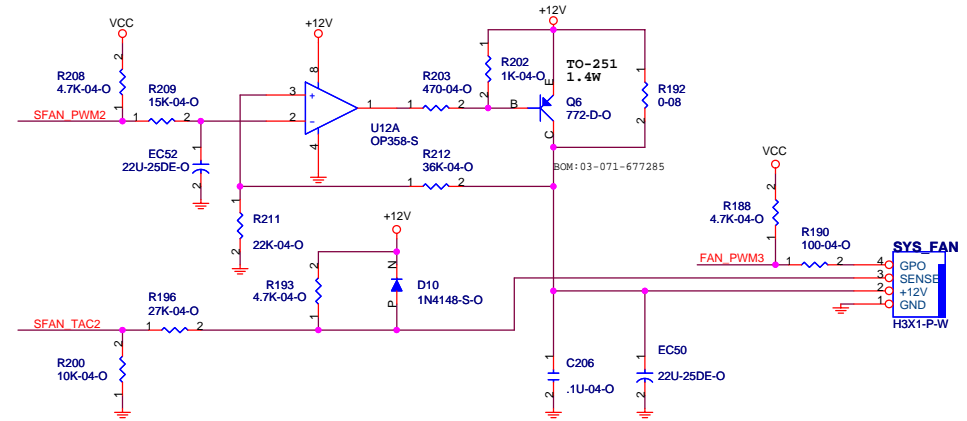
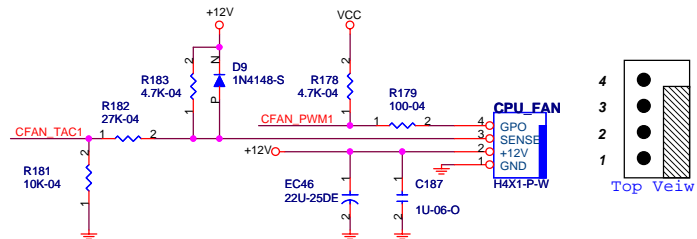
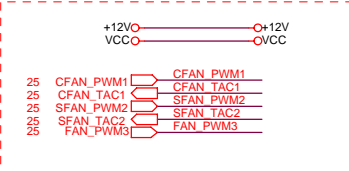
POWER CONNECTOR

External Connection

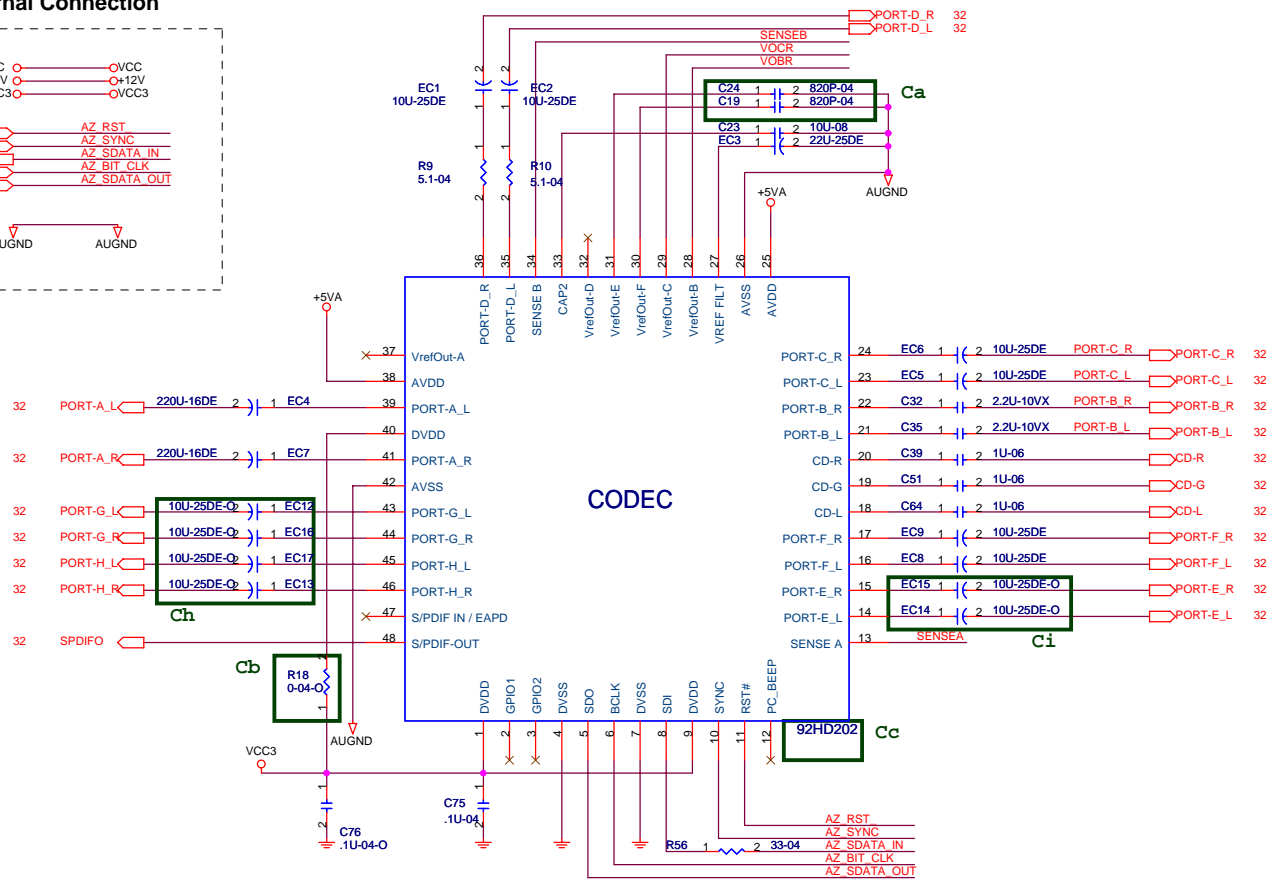
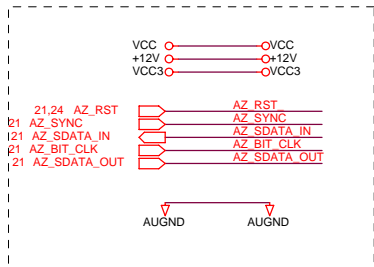


FAN

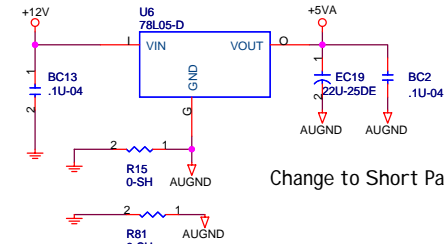
External Connection



External Connection

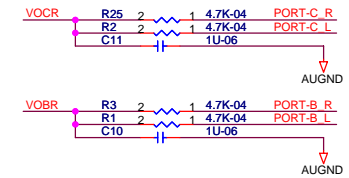


Analog Power

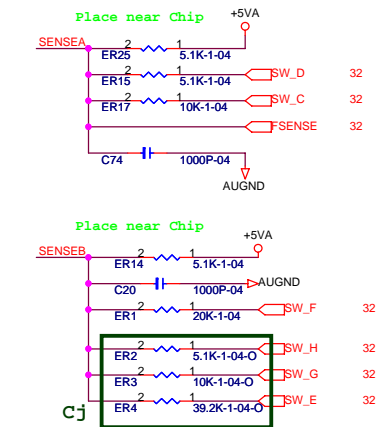


Change to Short Pad

MIC Bias



JD Resistors Networks



EMI Cap



Connection

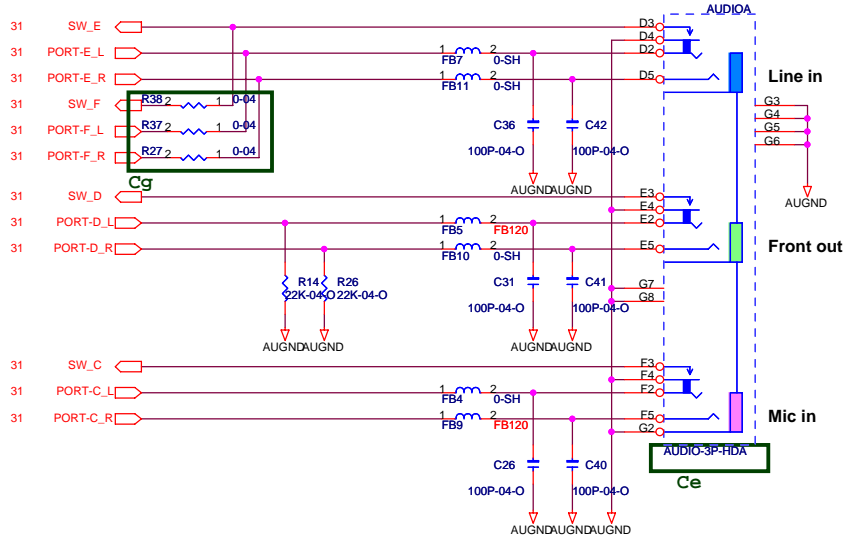
Port	pin	signal	206	202
	39,41	F-Line out	A	A
	21,22	F-Mic in	B	B
	23,24	R-Mic in	C	C
	35,36	R-Line out	D	D
	14,15	R-Surround	F	F
	16,17	R-Line in	E	F
	43,44	R-Cen/Bass	G	
	45,46	R-Side surr	H	
	18,20	CD In		
	48	SPDIF Out		

BOM Difference

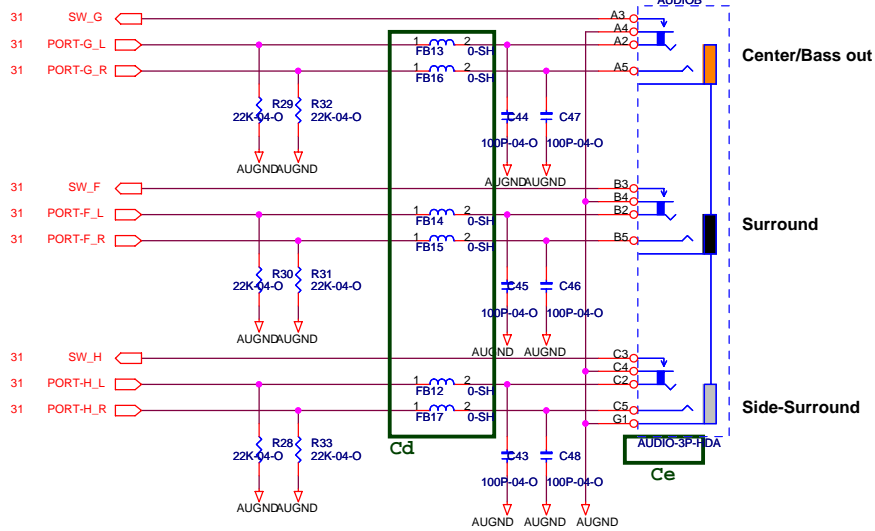
Location	92HD206 7.1 Ch	92HD202 5.1 CH
Ca	X	V
Cb	0-04	X
Cc	92H206	92HD202
Cd	V	X
Ce	AUDIO-6P	AUDIO-3P-HDA
Cg	X	V
Ch	V	X
Ci	V	X
Cj	V	X

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

REAR-AUDIO

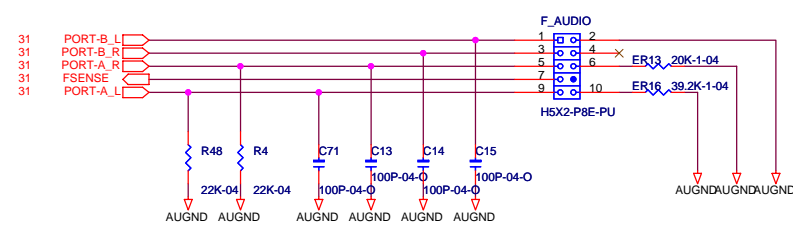


(Optional Rear Audio Panel)



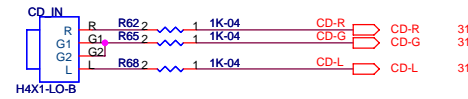
FRONT-AUDIO

Color:Purple



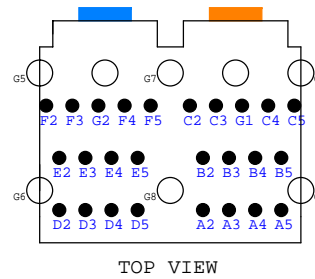
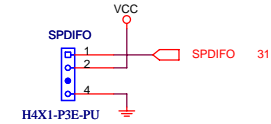
CD_IN

Color:Black

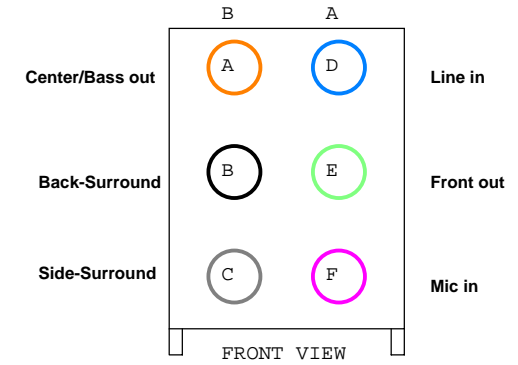


SPDIF-OUT

Color:Light Purple



TOP VIEW



ECS Elitegroup Computer Systems

Title				AUDIO AL888 (PANEL)	
Size	Document Number	RS740M-M			Rev
Custom					1.0
Date:	Monday, December 10, 2007	Sheet	32	of	35

ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

CPU PW
12V +/-5%

VRM SW
REGULATOR

VCORE(S0, S1)

VCC25A(S0,S1)

VTT_DDR (S0,S1,S3)

M2
VDDA 2.5V 0.1A
VDDCORE 0.8-1.55V 80A
DDRII MEM I/F VTT 0.125A, VDD 3A
VLDT 1.2V 0.5A

2.5V SHUNT
REGULATOR

VCC25A
(S0, S1)

VCC 1.2V SW
REGULATOR

VDDHT 1.2V (S0, S1)

VDDPCIE(S0, S1)

V_DIMM(S0,S1,S3)

VCC_NB (S0, S1)

1.8V LINEAR
REGULATOR

VDDL18&VDDLPT18(S0, S1)

VCC1.8(S0, S1)

VDDA18

VDD18

RS485/RS690
VDDHT 1.2V 0.5A
PCI-E CORE &VCO 2.25A
NB CORE VDDC 1.0-1.2V 5A
DAC 200mA LVDS 1.8V 300mA
PLL & DAC-Q 0.1A
PCI-E I/O 1500mA

5V_DUAL For V_DIMM(S0-->S5)

DUAL REGULATOR

1.8V VDD SW
REGULATOR

0.9V VTT_DDR
REGULATOR

VTT_DDR(S0,S1,S3)

DDRII DIMMs
VTT_DDR 2A
VDD MEM 12A

V_DIMM(S0,S1,S3)

+3.3VSB REGULATOR
ACPI CONTROLLER

3VSB (S0, S1, S3, S4, S5)

3VSB (S0, S1, S3, S4, S5)

VCC12_SB Linear
REGULATOR

1.2V STB LDO
REGULATOR

1.2VSB (S0, S1, S3, S4, S5)

VCC3(S0, S1)

SB600
X4 PCI-E 0.8A
ATA I/O 0.2A
ATA PLL 0.01A
PCI-E PVDD 80mA
SB CORE 0.6A
1.2V S5 PW 0.22A
3.3V S5 PW 0.01A
USB CORE I/O 0.2A
3.3V I/O 0.45A

Jumper Control USE 5VSB or VCC

5VA LDO
REGULATOR

+5VA (S0, S1,S3)

GBE
3.3V 0.5A (S0, S1)
3.3V 0.1A (S3)

SATA
3.3V 0.3A (S0, S1)

AC97/AZALIA
3.3V CORE 0.3A
5V ANALOG 0.1A

SUPER I/O
+5V SD 0.01A
+5V 0.1A

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X1 PCIE per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.1A


X16 PCIE	
3.3V	3.0A
12V	5.5A

USB X4 FR	
VDD	
5VDual	2.0A

USB X6 RL	
VDD	
5VDual	2.0A

2XPS/2	
5VDual	1.0A

3VSB (S0, S1, S3)


Elitegroup Computer Systems

Title

POWER DELIVERY CHART

Size Custom

Document Number **RS740M-M**

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Rev **1.0**

